

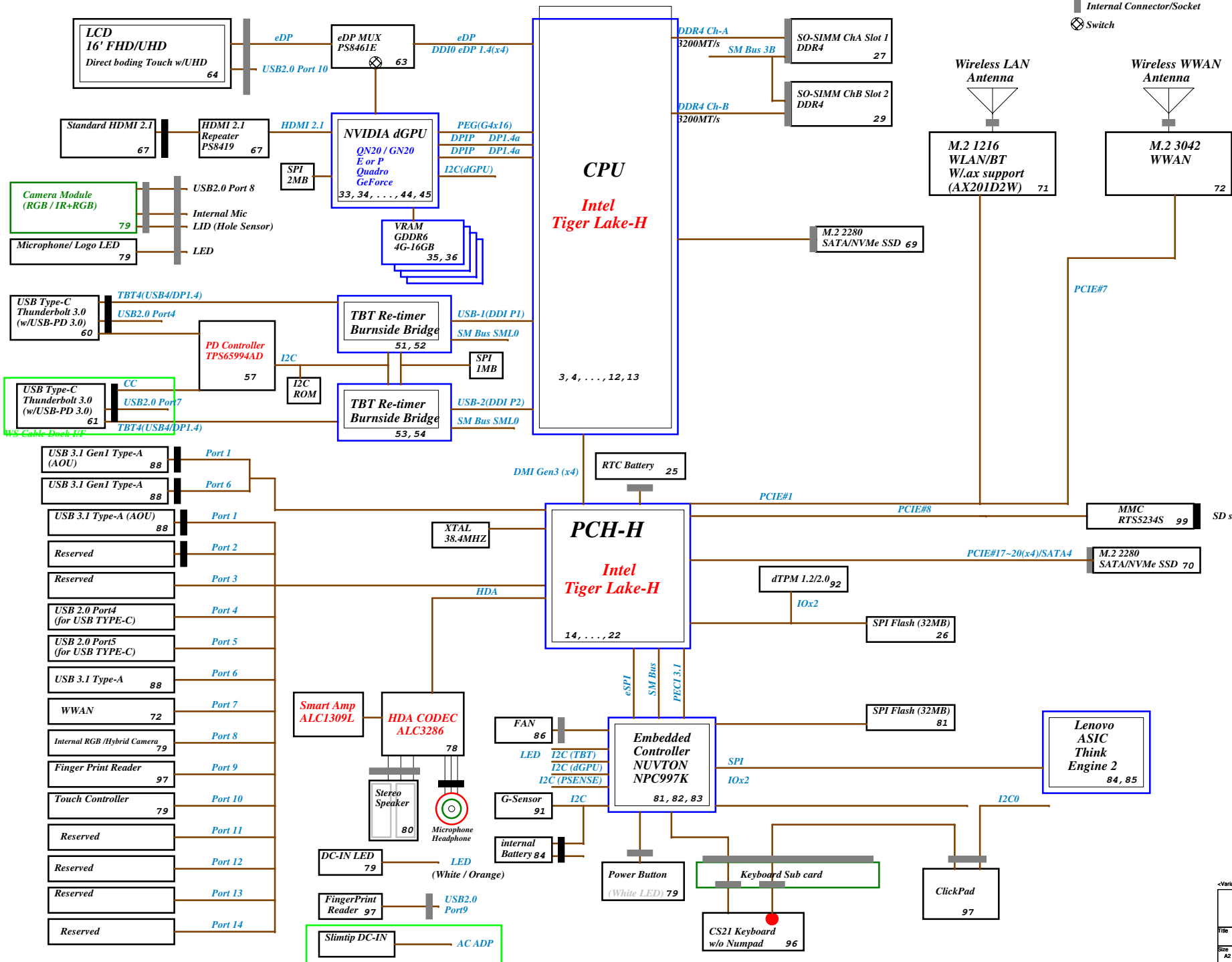
# Cheetah Schematic Page Number

001_TITLE PAGE	047_BLANK	093_SMBUS SWITCH/eSPI DEBUG	139_LOAD SW VCCST/VCCSTG
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003_SYSTEM DEFINED	049_BLANK	095_CAMERA/TOUCH/PWR BUTTON	141_LOAD TOUCH/SSD
004_CPU TGL-H : DDR4 CH-A	050_BLANK	096_KEYBOARD/TRACK POINT	142_LOAD SW B
005_CPU TGL-H : DDR4 CH-B	051_THUNDERBOLT RETIMER A (1/2)	097_CLICK PAD/FPR	143_LOAD SW WWAN&WLAN
006_CPU TGL-H : DDR CLK/DDI	052_THUNDERBOLT RETIMER A (2/2)	098_ME HOLE	144_LOAD BOM
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017_PCH TGL-H : GPIO (2/2)	063_eDP MUX	109_BLANK	
018_PCH TGL-H : PCIE/USB3	064_LCD CONNECTOR	110_DC/DC VCC5M/VCC3M	
019_PCH TGL-H : USB/SPI/MISC	065_BLANK	111_DC/DC VCC1R2A/VCC0R6B	
020_PCH TGL-H : POWER	066_BLANK	112_DC/DC VCC2R5A	
021_PCH TGL-H : GND	067_HDMI2.1 Retimer and CONN	113_BLANK	
022_PCH TGL-H : PCH Straps	068_BLANK	114_DC/DC IMVP9	
023_PCH TGL-H : BLANK	069_M.2 PCIE GEN4 SSD Slot	115_DC/DC VCCPUCORE	
024_PCH TGL-H : BLANK	070_M.2 PCIE GEN3 SSD Slot	116_BLANK	
025_RTC BATTERY	071_M.2 1216 MODULE	117_BLANK	
026_SPI FLASH	072_WWAN M.2 3042 SLOT	118_BLANK	
027_DDR4 CH-A	073_BLANK	119_VCCPUCORE DECOUPLING	
028_BLANK	074_BLANK	120_VCCCPUCORE_AUX	
029_DDR4 CH-B	075_BLANK	121_VCCCPUCORE_AUX	
030_BLANK	076_BLANK	122_DC/DC VCCGFXCORE_D IC	
031_BLANK	077_BLANK	123_DC/DC VCCGFXCORE_D1	
032_BLANK	078_AUDIO SIP (ALC3286)	124_BLANK	
033_N20P_PCI EXPRESS	079_SMATR AMP (ALC1309L)	125_VCC1R2VIDEO	
034_N20P_FB A/B	080_HP/MIC/SPEAKER/DEBUG PORT	126_VCC1R0VIDEO	
035_N20P_VRAM CH-A	081_NPCX997KA0BX(1/3)	127_LOAD SW VIDEO/3SUS	
036_N20P_VRAM CH-B	082_NPCX997KA0BX(2/3)	128_DISCHARGE Circuit VIDEO	
037_N20P_VRAM DECOUPLING	083_NPCX997KA0BX(3/3)	129_BLANK	
038_N20P_GPIO AND I2C	084_THINK ENGINE 2(1/2)	130_DC/DC VCC5_PD	
039_N20P_POWER	085_THINK ENGINE 2(2/2)	131_DC/DC VCC1R8_SUS	
040_N20P_GND	086_FAN CONNECTOR	132_BLANK	
041_N20P_DECOUPLING	087_MIPi60 DEBUG PORT	133_VCC12	
042_N20P_IFP A/B AND XTAL	088_USB POWER/CONNECTOR	134_BLANK	
043_N20P_MIO AND ROM	089_BLANK	135_BLANK	
044_N20P_IFP C/D AND E/F	090_BLANK	136_BLANK	
045_N20P_NCP45492	091_APS G-SENSOR	137_LOAD SW 1P8A	
046_BLANK	092_DISCRETE TPM 2.0	138_BLANK	



# Cheetah Block Diagram

Project Code: 4PD0NL010001  
PCB(Raw Card):213013-1



External Connector/Socket  
Internal Connector/Socket  
Switch

**PCB Layer Stackup**

10 Layers FR4

L1:Component  
L2:GND  
L3:Signal 1  
L4:VCC  
L5:Signal 2  
L6:Signal 3  
L7:VCC  
L8:Signal 4  
L9:GND  
L10:Component

**Battery Charger/Selector**

BQ24800RUYR 108

VINT20 M-BAT-PWR

**System DC/DC**

TPS51285B-1RUKR 110

VINT20 VCC5M VCC3M

**DC/DC VCC1R2A**

TPS51716RUKR 111

VINT20 VCC1R2A

**DC/DC VCC0R6B**

TPS51716RUKR 111

VINT20 VCC0R6B

**DC/DC VCC2R5A**

NB695GD-C669-Z 112

VINT20 VCC2R5A

**DC/DC IMVP9**

NCP81305MINTXG 114

VINT20 VCCCPUCORE

**DC/DC VCCCPUCORE\_AUX**

NCP81269MINTXG 120

VINT20 VCCCPUCORE\_AUX

**DC/DC VCCPCHCORE**

NCP81269MINTXG 121

VINT20 VCCPCHCORE

**DC/DC VCCGFXCORE\_D**

NCP81611AMNTXG 122

VGA\_IN VCCPGFXCORE\_D

**DC/DC VCCIR2VIDEO**

NCP81278TMNTXG 125

VINT20\_VGA VCCIR2VIDEO

**DC/DC VCCIR0VIDEO**

NB694GD-C669-Z 126

VINT20 VCCIR0VIDEO

**DC/DC VCC5\_PD**

NB693GQ-C669-Z 130

VINT20 VCC5\_PD

**DC/DC VCC1R8\_SUS**

NB693GQ-C669-Z 131

VINT20 VCC1R8\_SUS

**DC/DC VCC12**

MP3431GL-C669-Z 133

VCC5M VCC12

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**BLOCK DIAGRAM**

Cheetah

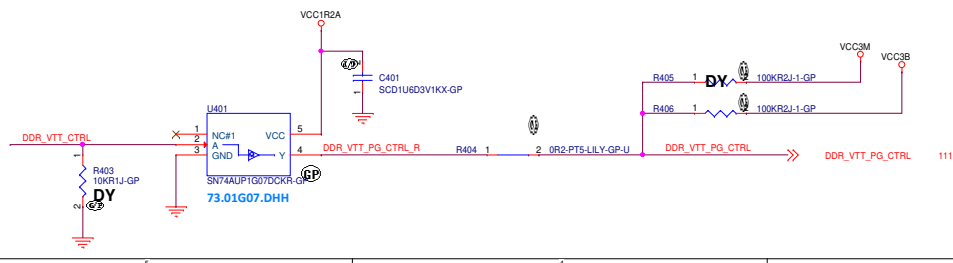
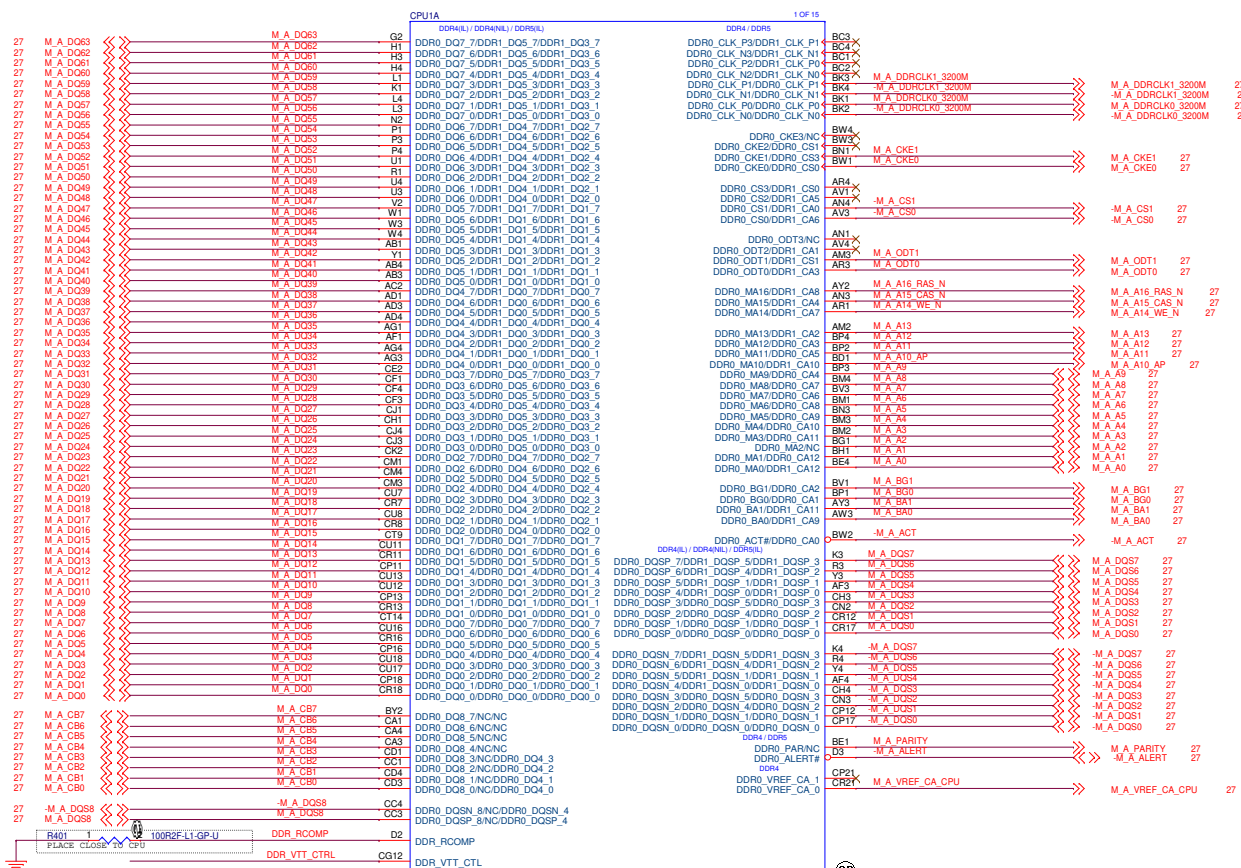
Rev -1

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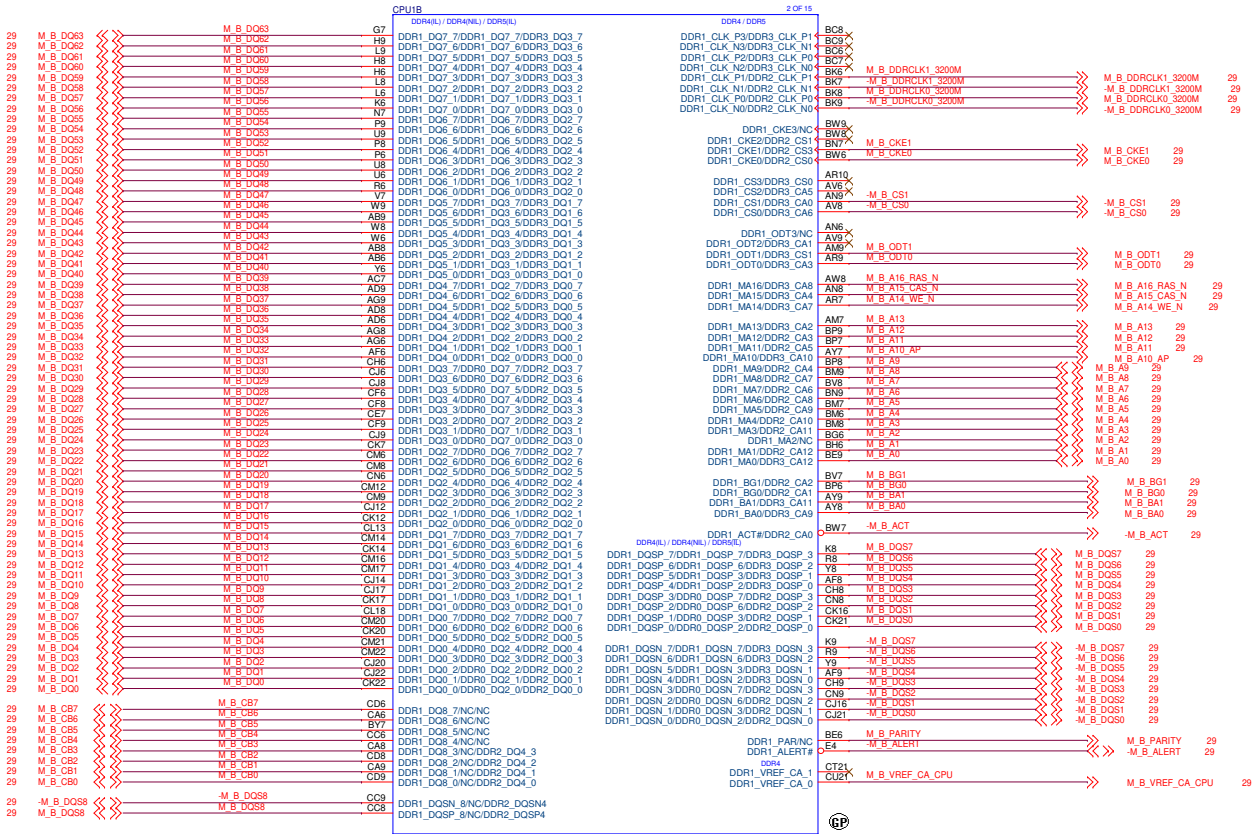




















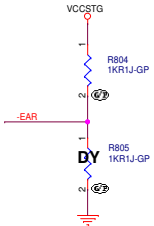
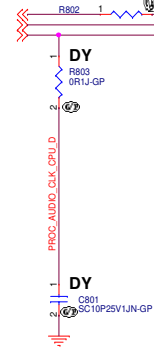


CPU

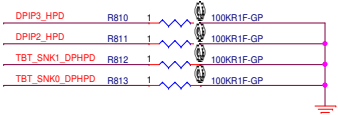
TBT PortA  
(JTBT1)

TBT PortB  
(JTBT2)

17 PROC\_AUDIO\_SDI\_CPU  
17 PROC\_AUDIO\_SDO\_CPU  
17 PROC\_AUDIO\_CLK\_CPU

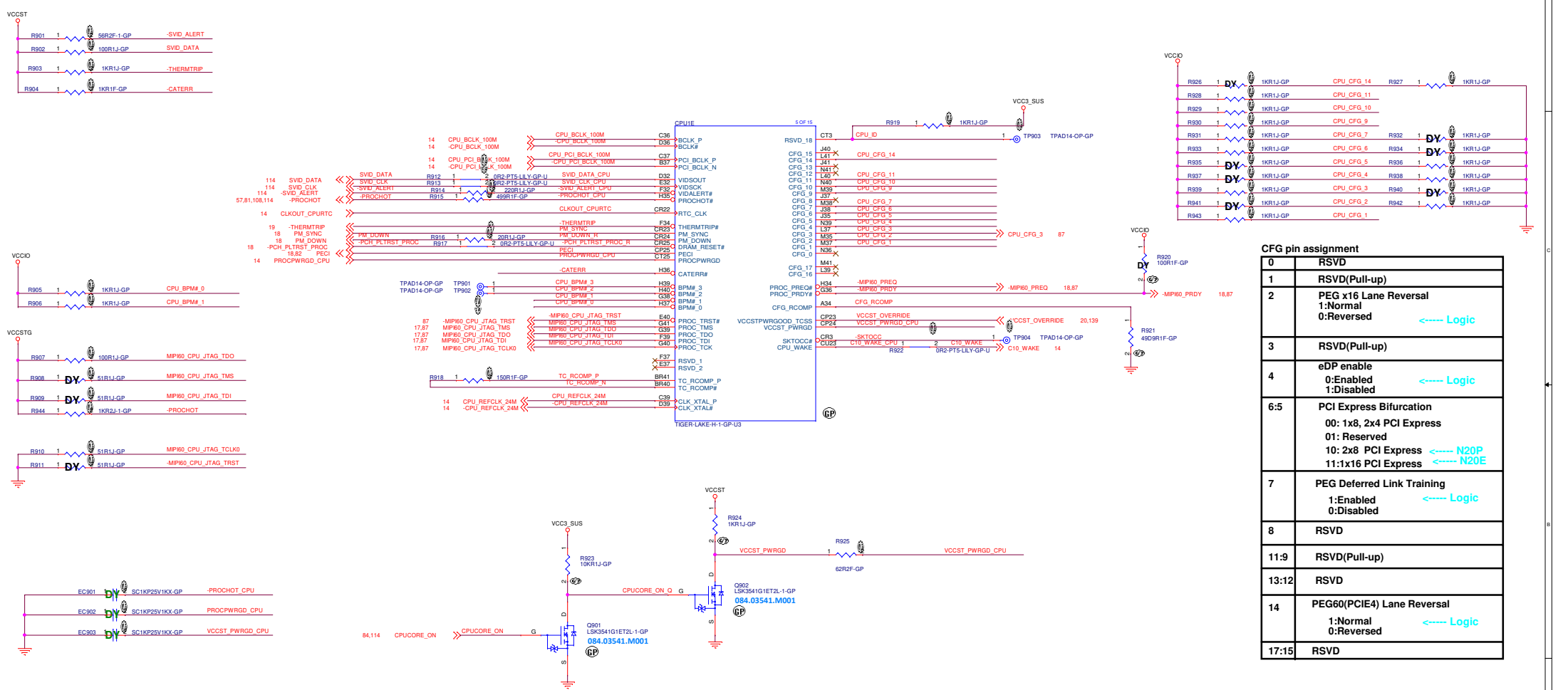


-EAR pin assignment  
Stall reset sequence after PCU PLL lock until de-asserted  
1: Normal(No stall)  
0: Stall





CPU



CFG pin assignment	
0	RSVD
1	RSVD(Pull-up)
2	PEG x16 Lane Reversal 1:Normal 0:Reversed <div>----- Logic</div>
3	RSVD(Pull-up)
4	eDP enable 0:Enabled 1:Disabled <div>----- Logic</div>
6.5	PCI Express Bifurcation 00: 1x8, 2x4 PCI Express 01: Reserved 10: 2x8 PCI Express 11: 1x16 PCI Express <div>----- N20P ----- N20E</div>
7	PEG Deferred Link Training 1:Enabled 0:Disabled <div>----- Logic</div>
8	RSVD
11:9	RSVD(Pull-up)
13:12	RSVD
14	PEG60(PCIe4) Lane Reversal 1:Normal 0:Reversed <div>----- Logic</div>
17:15	RSVD

VCCST\_PWRGD requirements

- 1) Indication that the VCCST/VDDQ power supplies are stable and within specification
- 2) VCCST\_PWRGD must go low during Sx pwr states, regardless of the voltage level of VCCST
- 3) VCCST\_PWRGD can assert before or equal to PCH\_PWROK, but must never lag it.

If VCCSTG is used instead of VCC1R05\_SUS, VCCST\_PWRGD will be off in Sleep S0 because VCCSTG may be turned off when in Sleep S0. Currently, VCCSTG is still on in Sleep S0 but we may change logic to turn off VCCSTG in sleep S0. (CT\_20141216)



NCTF\_CPU\_LR\_1

NCTF\_CPU\_LL\_2

NCTF\_CPU\_UL\_1

NCTF\_CPU\_LR\_2

NCTF\_CPU\_UL\_2

NCTF\_CPU\_UR\_1

NCTF\_CPU\_UR\_2

NCTF\_CPU\_UL\_1 1 TP1001 TPAD14-OP-GP  
NCTF\_CPU\_UL\_2 1 TP1002 TPAD14-OP-GP  
NCTF\_CPU\_LL\_1 1 TP1003 TPAD14-OP-GP  
NCTF\_CPU\_LL\_2 1 TP1004 TPAD14-OP-GP

NCTF\_CPU\_UR\_1 1 TP1005 TPAD14-OP-GP  
NCTF\_CPU\_UR\_2 1 TP1006 TPAD14-OP-GP  
NCTF\_CPU\_UR\_1 1 TP1007 TPAD14-OP-GP  
NCTF\_CPU\_LL\_2 1 TP1008 TPAD14-OP-GP

BOM1

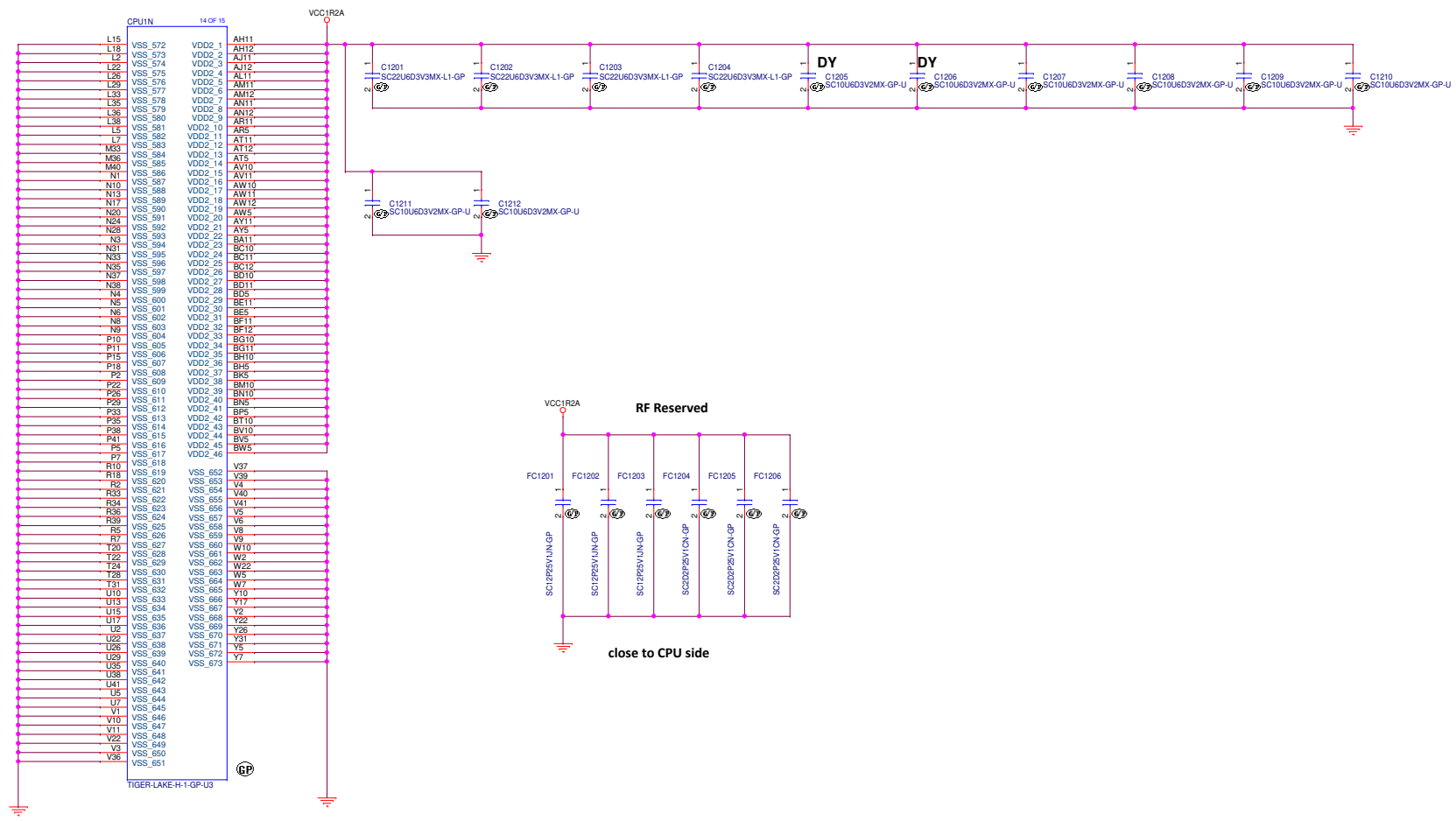
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File CPU TGL-H GND  
Size C Document Number Cheetah Rev -1  
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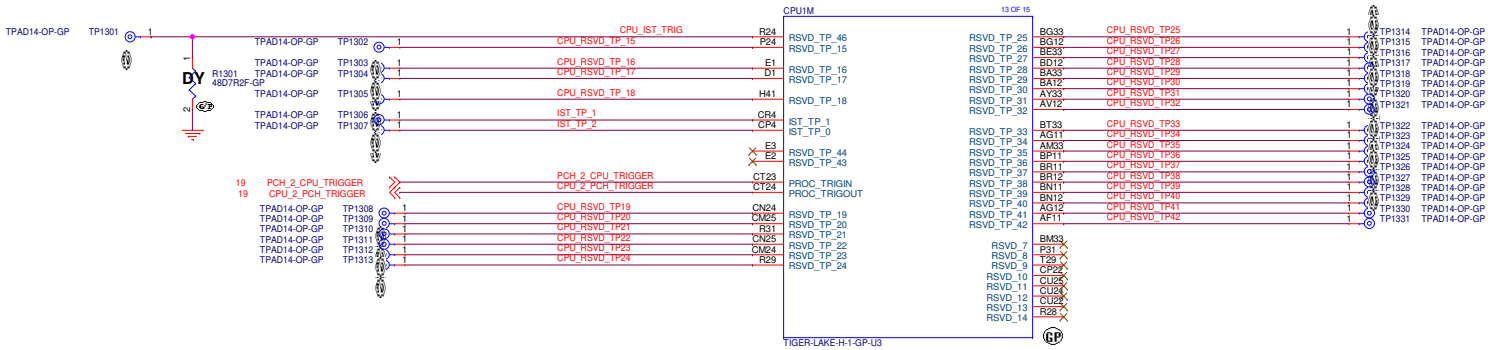




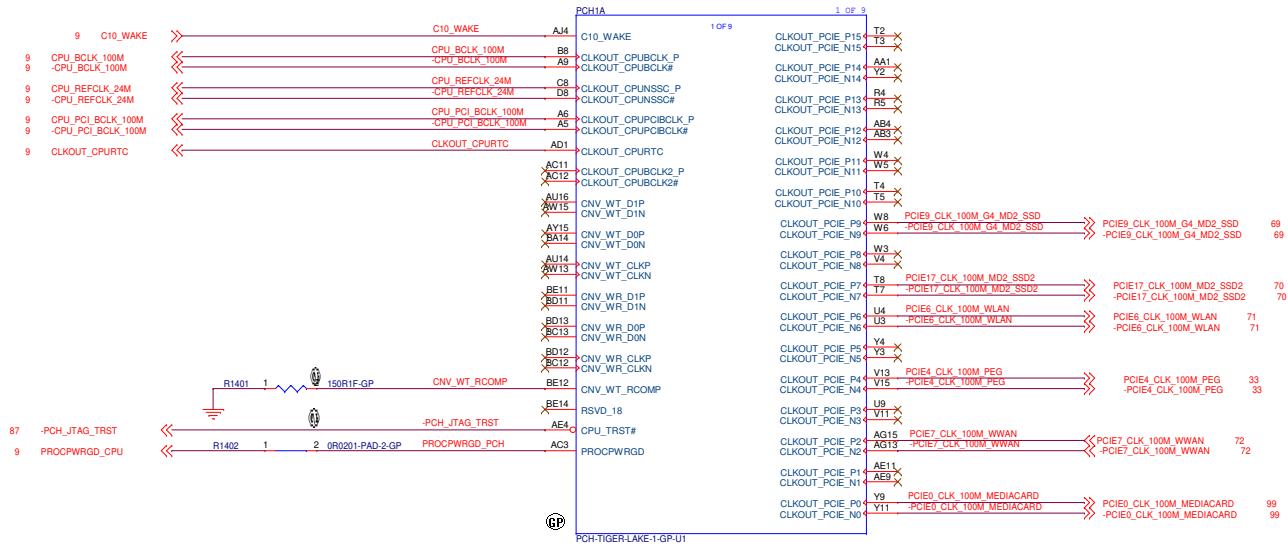




CPU



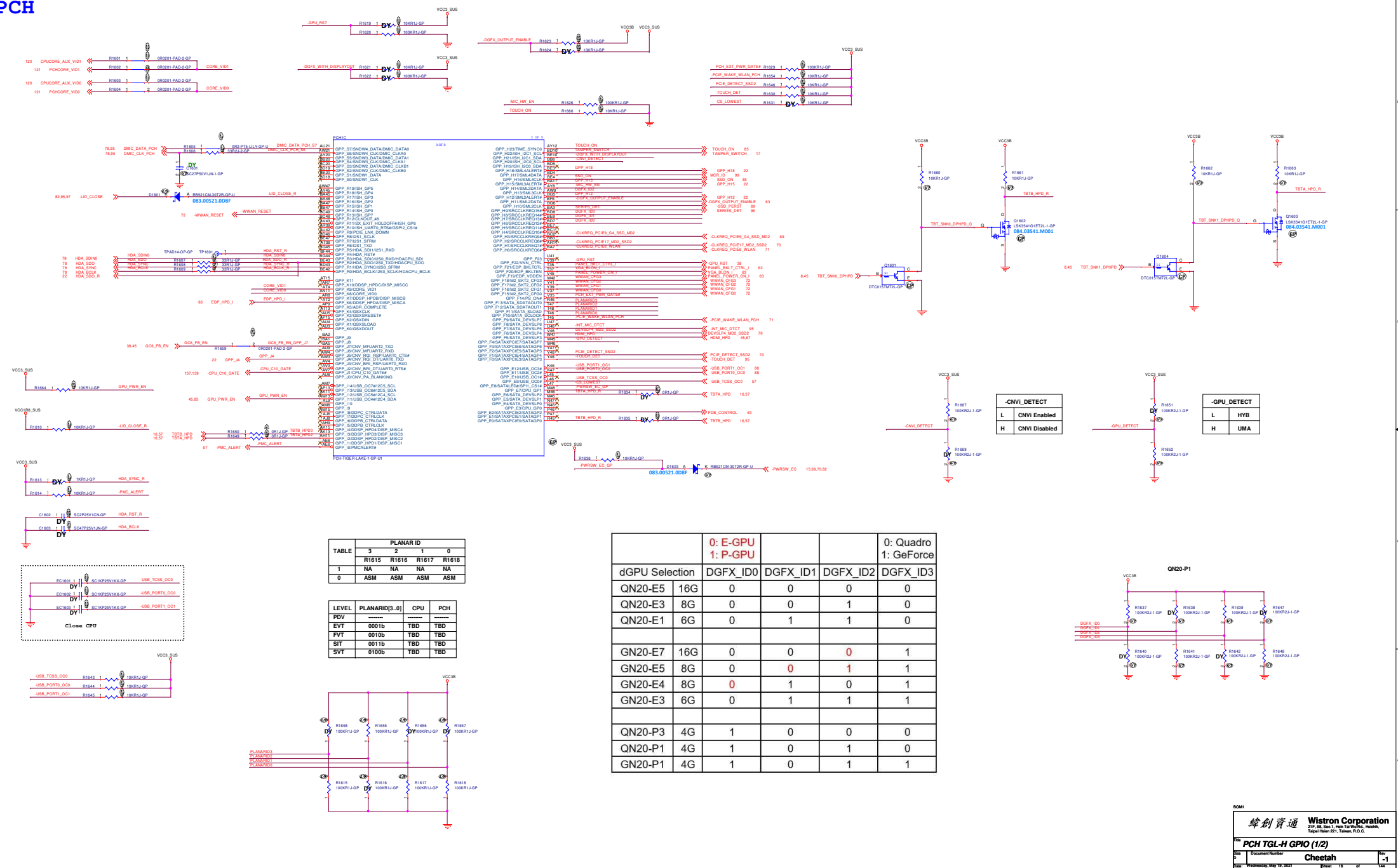








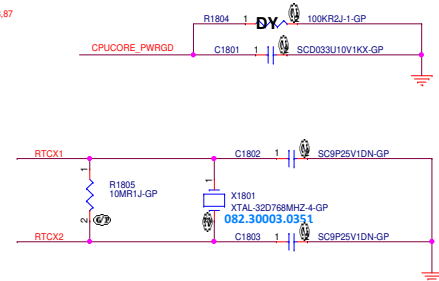






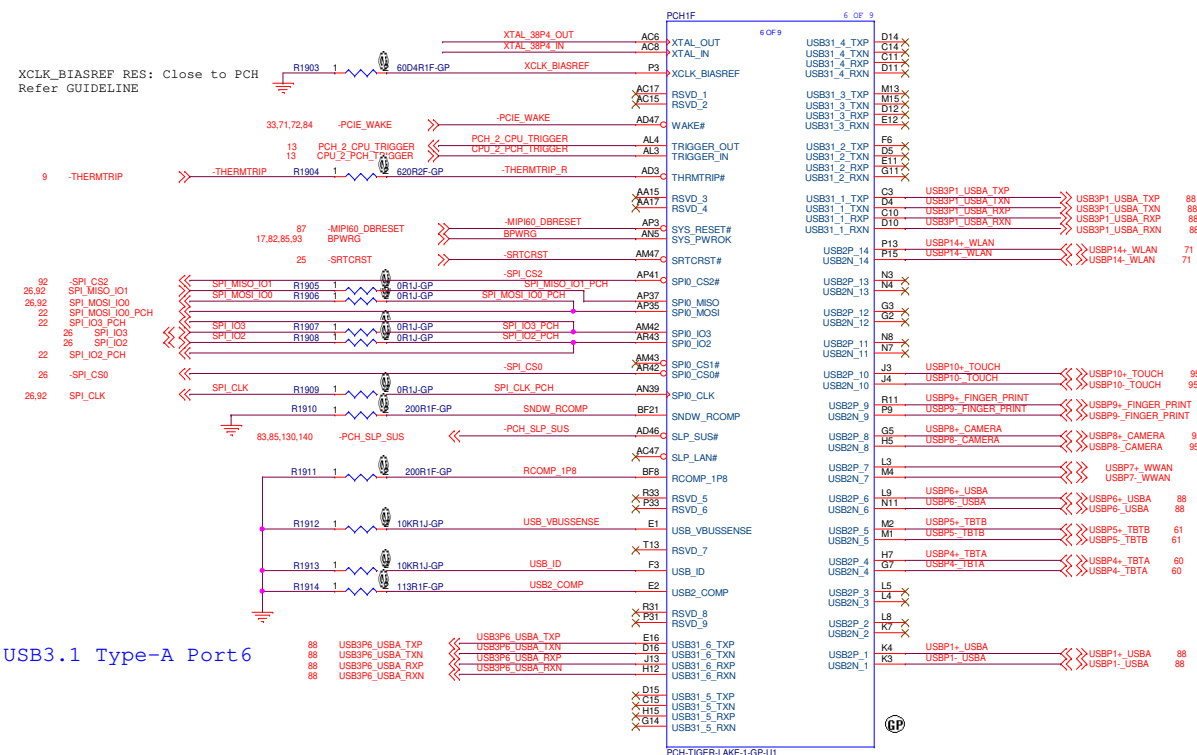
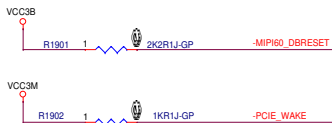








# PCH



USB3.1 Type-A Port1 (AOU)

WLAN

TOUCH

97 Finger print

CCD

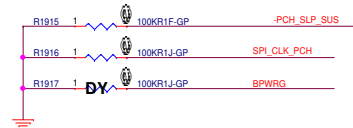
WWAN

USB Type-A #3

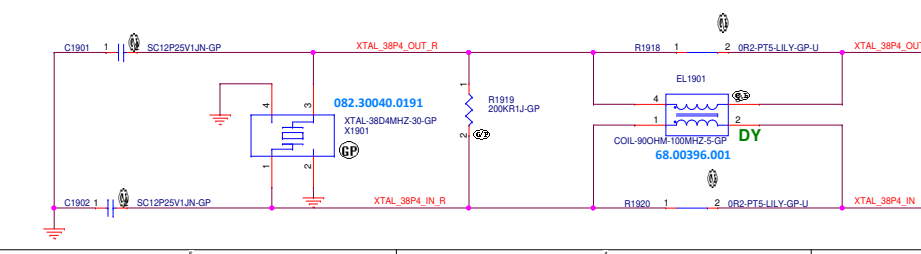
TBT PortB

TBT PortA

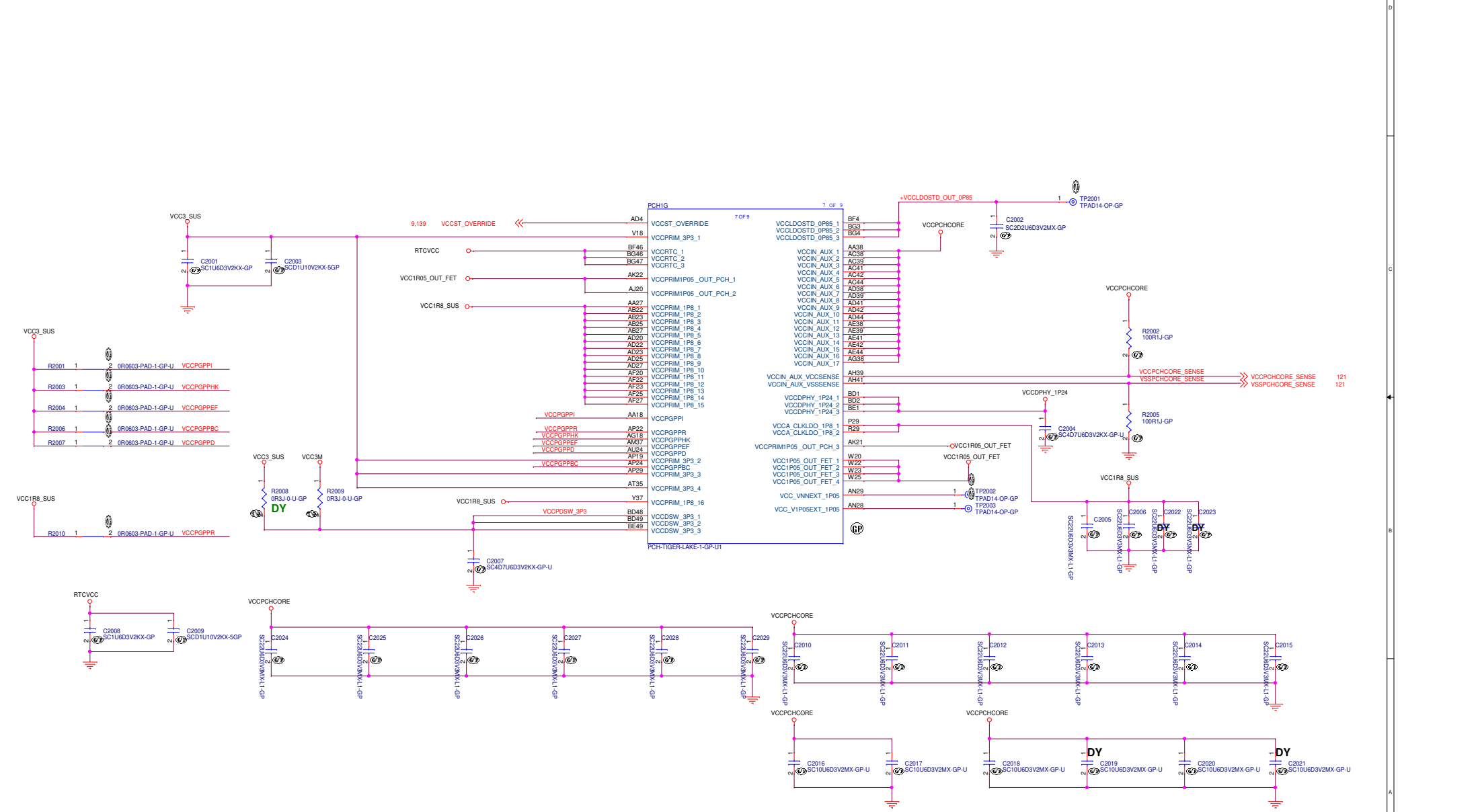
USB Type-A #1



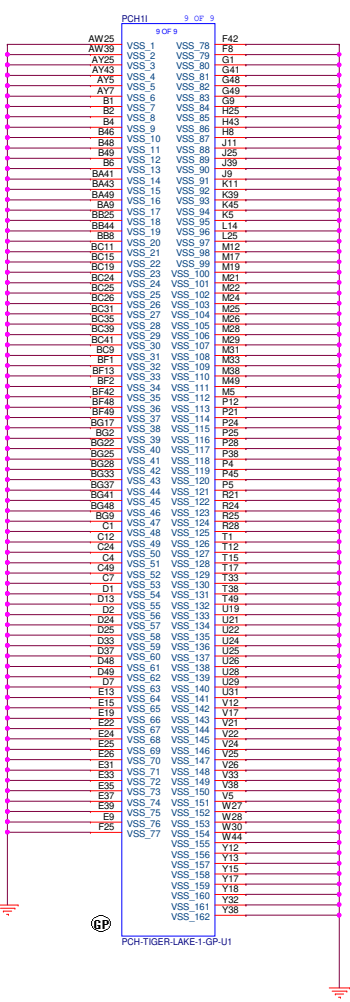
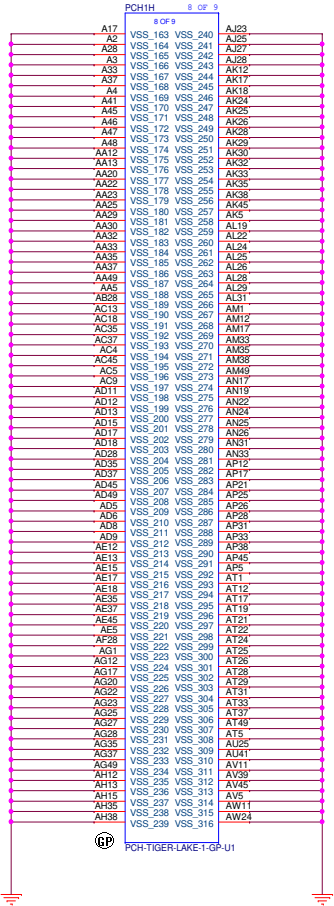
# PCH Crystal













# PCH Straps

Reference 615985-tgl-rkl-pch-eds-vol1-rev0p7, Table17

Signal	Usage	Comment	Setting
GPP_B14/SPKR	Top Swap Override	0 = Disable "TOP Swap" Mode (Default) 1 = Enable "TOP Swap" Mode This strap has a 20k internal PD	This strap is set by EC. See "BIOS_HEALING" signal
GPP_B18/GSPI0_MOSI	No Reboot	0 = Disable "No Reboot" Mode (Default ) 1 = Enable "No Reboot" Mode This strap has a 20k internal PD	17 GPP_B18_NO_REBOOT >> GPP_B18_NO_REBOOT R2201 1 DY 1KR1J-GP >VCC3_SUS
GPP_C2/SMBALERT#	TLS Confidentiality	0 = Disable ME Crypto TLS(Default) 1 = Enable ME Crypto TLS with Confidentiality This strap has a 20k internal PD	17 GPP_C2 >> GPP_C2 R2202 1 4K7R1J-GP >VCC3_SUS
GPP_C5/SML0ALERT#	eSPI Disable	0 = Enable eSPI (Default) 1 = Disable eSPI This strap has a 20k internal PD	17 GPP_C5 >> GPP_C5 R2203 1 DY 4K7R1J-GP >VCC3_SUS
SPI0_MOSI	Reserved	External pull-up is required Recommend 4.7K PU	19 SPI_MOSI_I00_PCH >> SPI_MOSI_I00_PCH R2204 1 4K7R1J-GP >VCC3_SUS
GPP_G9/ISH_SPI_CLK/ DDP3_CTRLDATA/ GSPi2_CLK/ TBT_LSX2_RXD	DDP3 I2C/TBT_LSX2/ BBSB_LS2 pins VCC configuration	0 = DDP3 I2C/TBT_LSX2/BBSB_LS2 pins at 1.8V 1 = DDP3 I2C/TBT_LSX2/BBSB_LS2_TX pins at 3.3V This strap has a 20k internal PD	17,53 TBT_LSX2_RXD >> TBT_LSX2_RXD R2205 1 DY 4K7R1J-GP >VCC3_SUS
GPP_G11/ ISH_SPI_MOSI/ DDP4_CTRLDATA/ GSPi2_MOSI/ TBT_LSX3_RXD	DDP4 I2 /TBT_LSX3/ BSSB_LS3 pins VCC configuration	0 = DDP4 I2C/TBT_LSX3/BBSB_LS3 pins at 1.8V 1 = DDP4 I2C/TBT_LSX3/BBSB_LS3 pins at 3.3V This strap has a 20k internal PD	NC
GPP_B23/ SML1ALERT#/ PCHHOT#	CPUNSSC Clock Frequency	0 = 38.4 MHz clock (direct from crystal) (Default) 1 = 19.2 MHz clock (derived from 38.4 MHz crystal) This strap has a 20k internal PD	17 GPP_B23 >> GPP_B23 R2206 1 DY 4K7R1J-GP >VCC3_SUS
SPI0_IO2	Reserved	External pull-up is required Recommend 100K if pulled up to 3.3V	19 SPI_IO2_PCH >> SPI_IO2_PCH R2207 1 100KR1J-GP >VCC3_SUS
SPI0_IO3	Reserved	External pull-up is required Recommend 100K if pulled up to 3.3V	19 SPI_IO3_PCH >> SPI_IO3_PCH R2208 1 100KR1J-GP >VCC3_SUS
GPP_R2 / HDA_SDO / I2S0_TXD	Flash Descriptor Security Override	0 = Enable security measures defined in the Flash Descriptor (Default) 1 = Disable Flash Descriptor Security (override) This strap has a 20k internal PD	VCC3_SUS PLACE ON BOTTOM SIDE TEST PAD BOTTOM SIDE DO NOT MOVE AFTER FIX R2209 1 1KR1J-GP 911_9453 R2210 1 DY 0R1J-GP TPAD14-OP-GP TPAD14-OP-GP HDA_SDO_R << HDA_SDO_R 16
GPP_H12/ SML2ALERT#	eSPI Flash Sharing Mode	0 = Master Attached Flash Sharing (MAFS) enabled (Default) 1 = Slave Attached Flash Sharing (SAFS) enabled This strap has a 20k internal PD	16 GPP_H12 >> GPP_H12 R2211 1 DY 4K7R1J-GP >VCC3_SUS
GPP_H15 / SML3ALERT#	JTAG ODT Disable	0 = JTAG ODT is disabled (Default) 1 = JTAG ODT is enabled This strap has a 20k internal PD	16 GPP_H15 >> GPP_H15 R2212 1 100KR1J-GP >VCC3_SUS
GPP_H18 / SML4ALERT#	VCCSPI Voltage Configuration	0 = VCCSPI at 3.3 V (Default) 1 = VCCSPI at 1.8 V This strap has a 20k internal PD	16 GPP_H18 >> GPP_H18 R2213 1 DY 4K7R1J-GP >VCC3_SUS
GPP_G13 / DDP1_CTRLDATA / TBT_LSX0_RXD	DDP1 I2C/TBT_LSX0 / BSSB_LS0 pins VCC configuration	0 = DDP1 I2C / TBT_LSX0 / BSSB_LS0 pins at 1.8V 1 = DDP1 I2C / TBT_LSX0 / BSSB_LS0 pins at 3.3V This strap has a 20k internal PD	NC
GPP_G15 / DDP2_CTRLDATA / TBT_LSX1_RXD	DDP2 I2C /TBT_LSX1 / BSSB_LS01pins VCC configuration	0 = DDP2 I2C / TBT_LSX1 / BSSB_LS1 pins at 1.8V 1 = DDP2 I2C / TBT_LSX1 / BSSB_LS1 pins at 3.3V This strap has a 20k internal PD	17,51 TBT_LSX1_RXD >> TBT_LSX1_RXD R2214 1 DY 4K7R1J-GP >VCC3_SUS
DBG_PMODE	Reserved	This strap should sample high This strap has a 20k internal PU	NC
GPP_J2 / CNV_BRI_DT / UART0_RTS#	XTAL Frequency Selection	0 = 38.4 MHz (Default) 1 = 24 MHz This strap has a 20k internal PD	
GPP_J4 / CNV_RGI_DT / UART0_TXD	M.2 CNVi Mode Select	0 = Integrated CNVi enabled 1 = Integrated CNVi disabled This strap doesn't have an internal PU or PD. A weak external pull-up is required.	16 GPP_J4 >> GPP_J4 R2217 1 100KR1J-GP >VCC1R8_SUS
GPP_B22 / GSPi1_MOSI	Boot BIOS Strap (BBS)	0 = BIOS fetches are routed to SPI (MAF) or the eSPI Flash Channel (SAF) 1 = BIOS fetches are routed to the eSPI Peripheral Channel This strap has a 20k internal PD	17 GPP_B22 >> GPP_B22 R2216 1 DY 4K7R1J-GP >VCC3_SUS
GPD7	Reserved	This strap should sample LOW This strap has a 20k internal PD	NC(Used only as GPIO)



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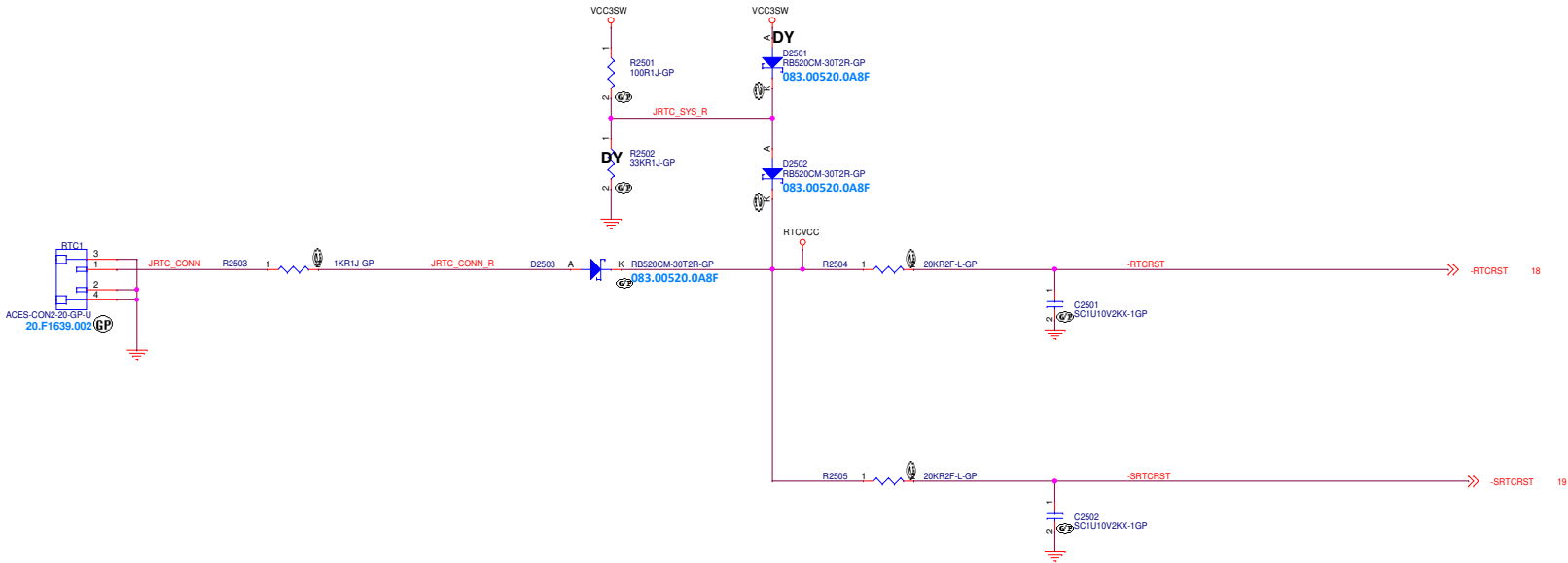
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-1

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PCH SPI FLASH

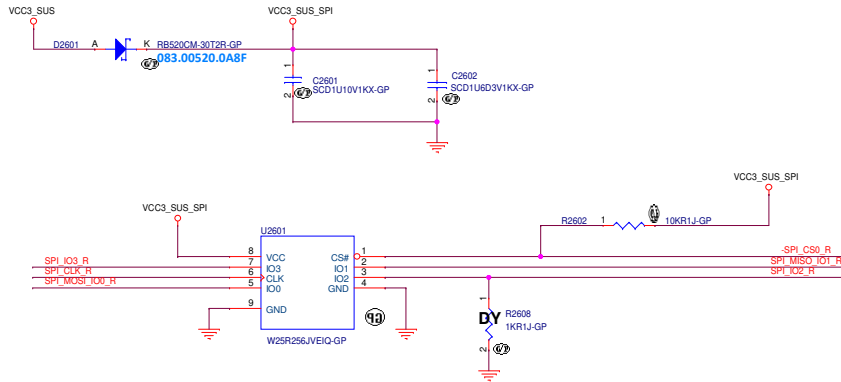


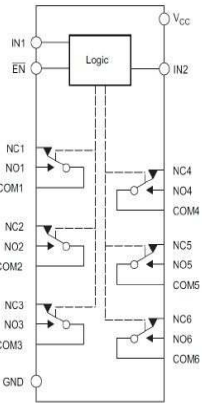
TABLE of SPI U2601 (32MB SOIC8/WSON)		
VENDOR	P/N	Wistron P/N
WINBOND	W25R256JVEIQ-GP(WSON)	072.25256.0L01
MACRONIX	MX77L25650FZ4I42	072.77256.0003
GIGADEVICE	GD25R256DYIGR	072.25256.0H03

WSON Design



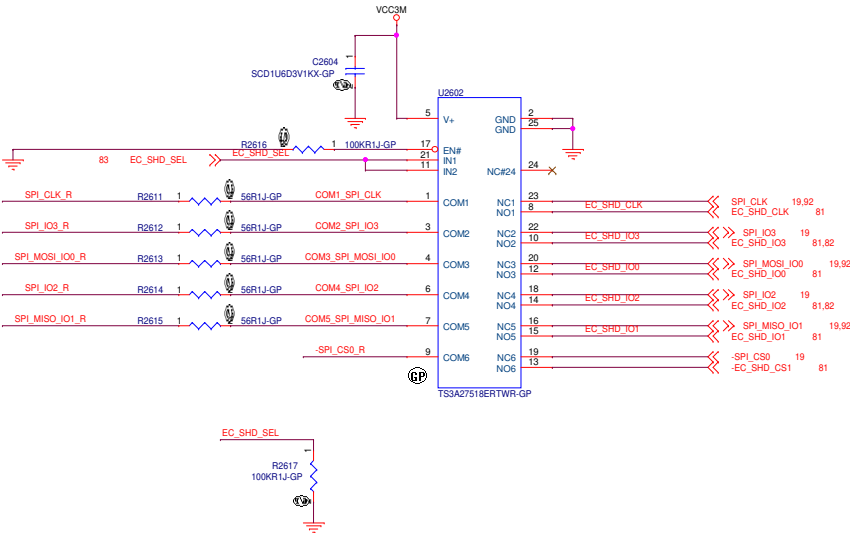
SPI Switch

Functional Block Diagram



Function Table

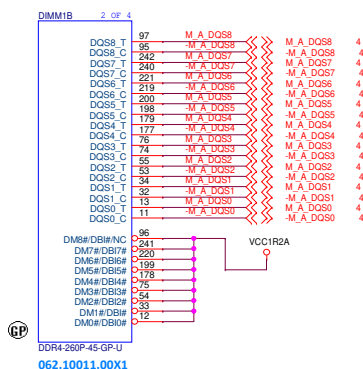
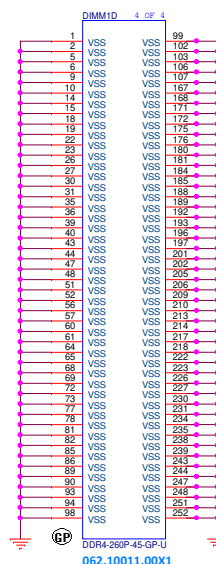
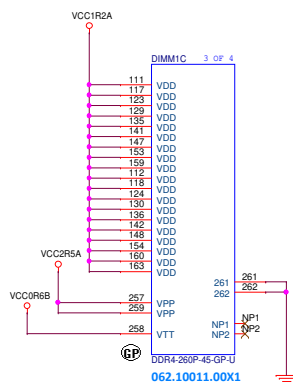
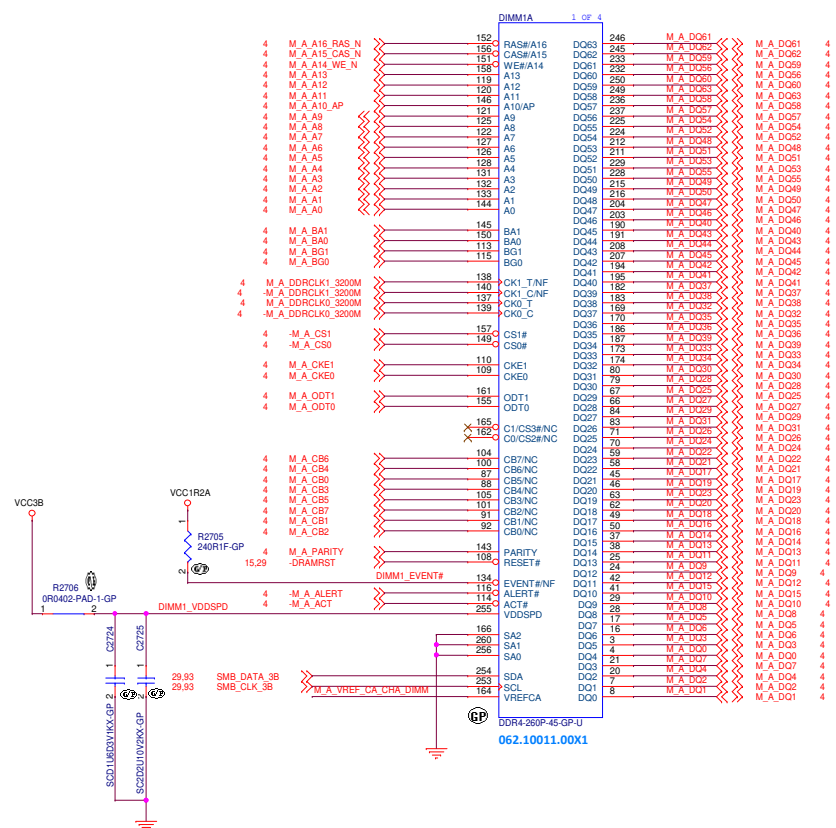
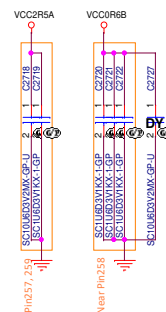
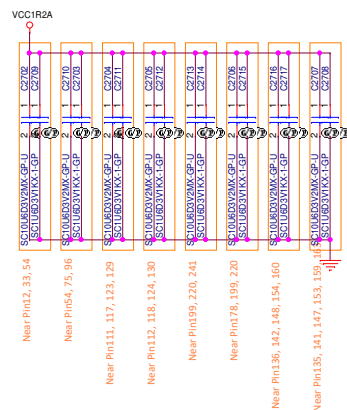
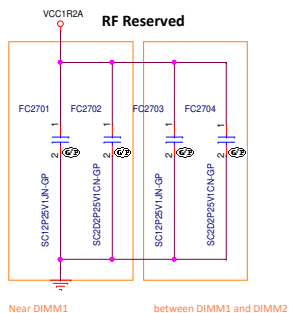
EN	IN1	IN2	NC1/2/3 TO COM1/2/3, COM1/2/3 TO NC1/2/3	NC4/5/6 TO COM4/5/6, COM4/5/6 TO NC4/5/6	NO1/2/3 TO COM1/2/3, COM1/2/3 TO NO1/2/3	NO4/5/6 TO COM4/5/6, COM4/5/6 TO NO4/5/6
H	X	X	OFF	OFF	OFF	OFF
L	L	L	ON	ON	OFF	OFF
L	H	L	OFF	ON	ON	OFF
L	L	H	ON	OFF	OFF	ON
L	H	H	OFF	OFF	ON	ON



From PCH SPI I/F

From EC SPI I/F







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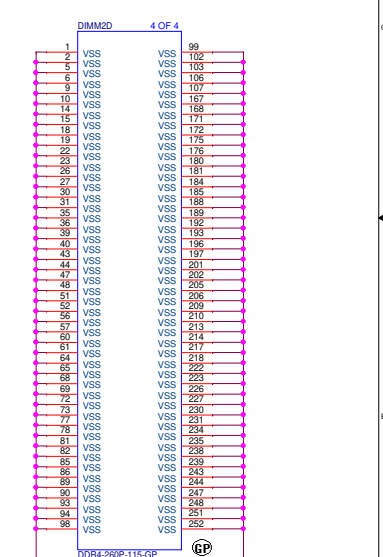
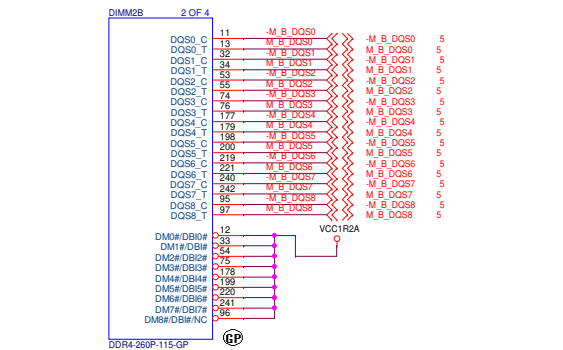
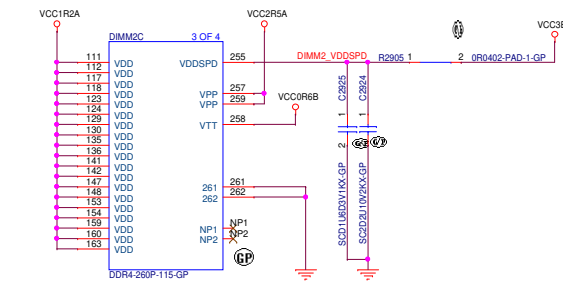
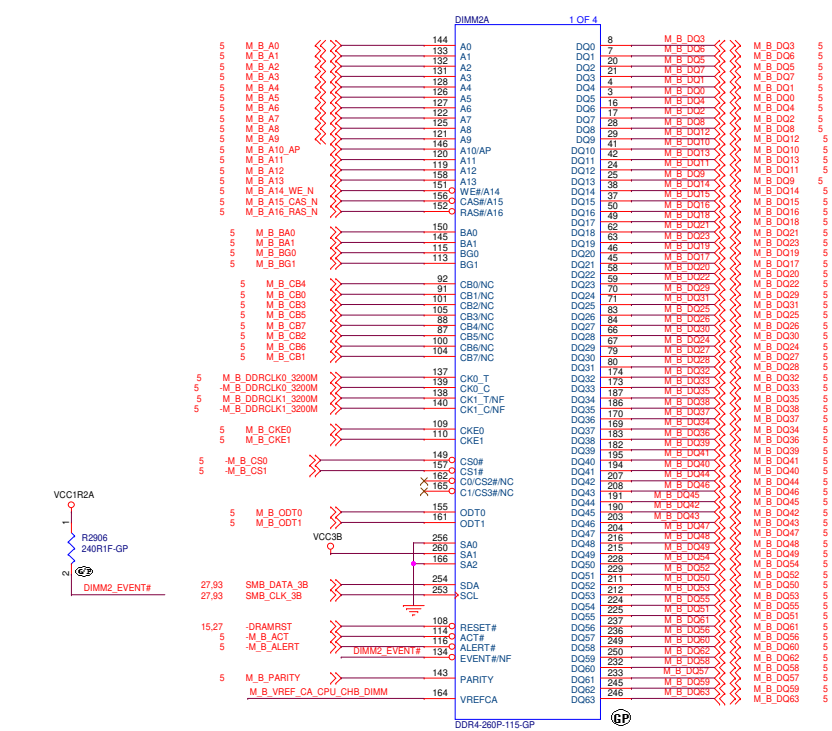
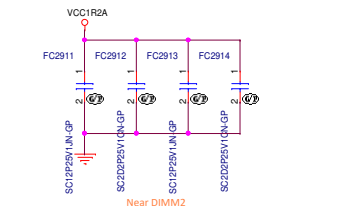
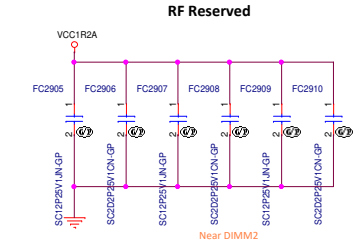
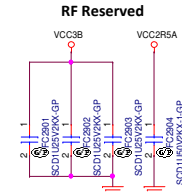
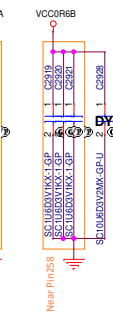
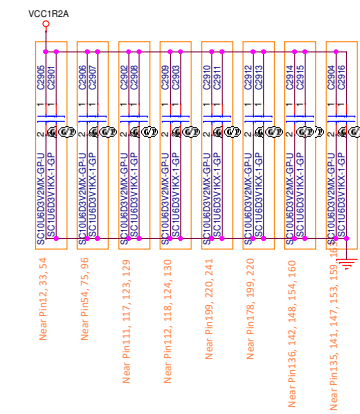
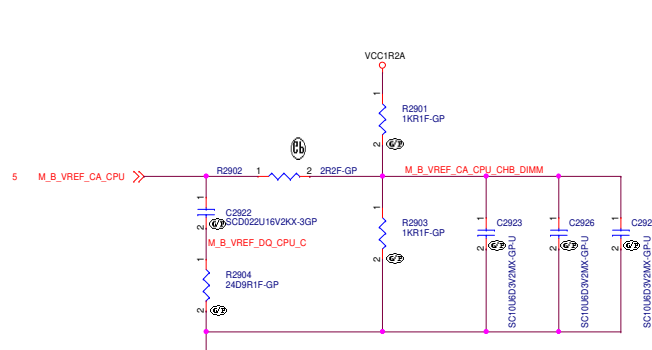
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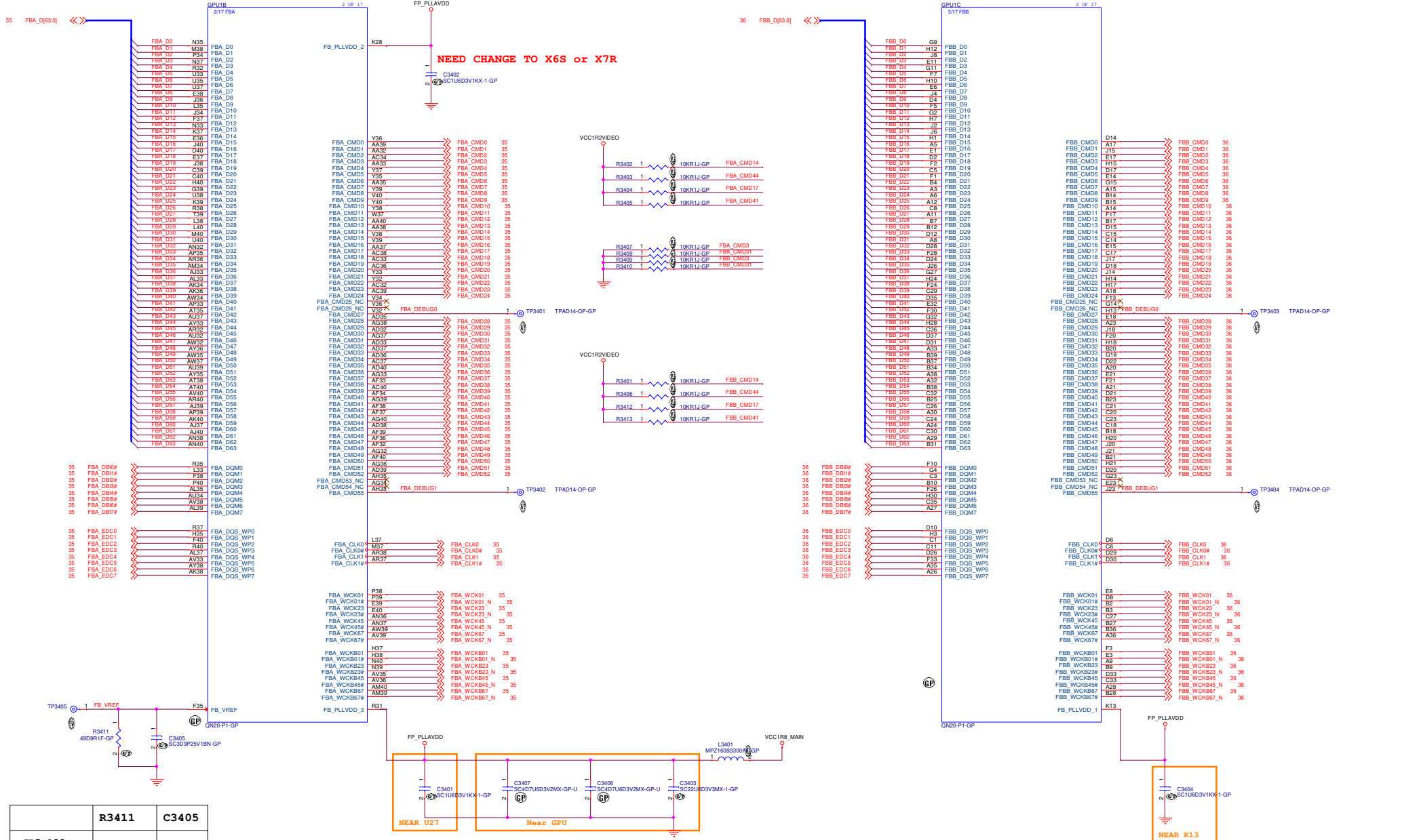
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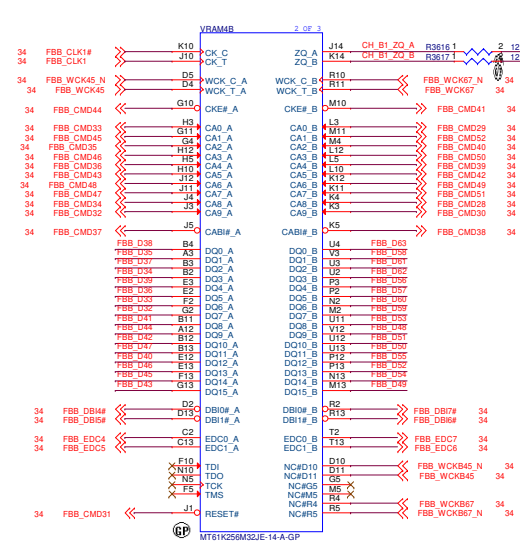
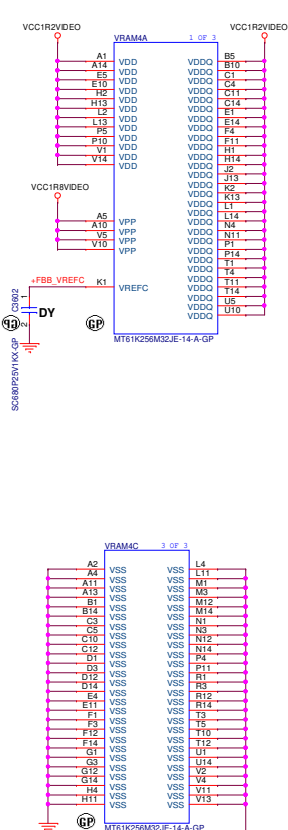
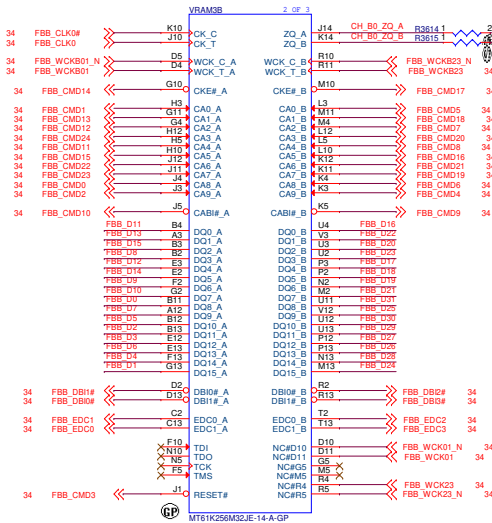
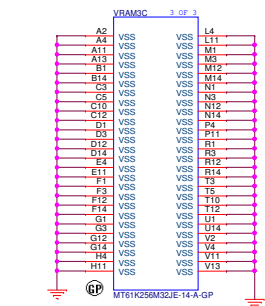


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GB5-128 (QN20P-Q1)	49.9 ohm	ASM
GB5B-128 (QN20P-Q3)	2.49K ohm	ASM

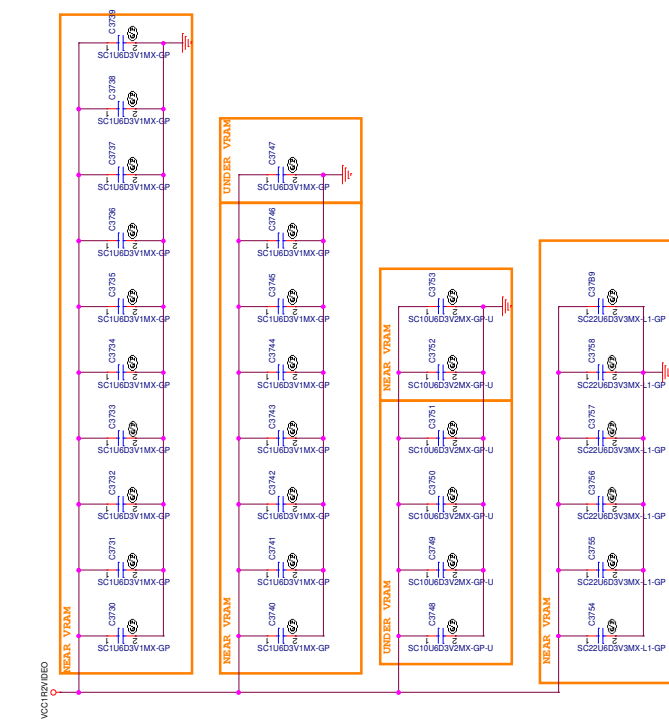
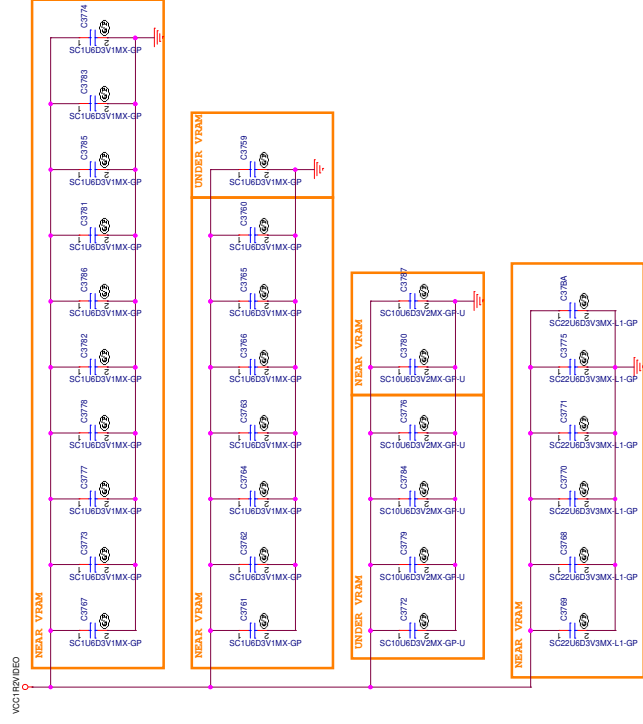
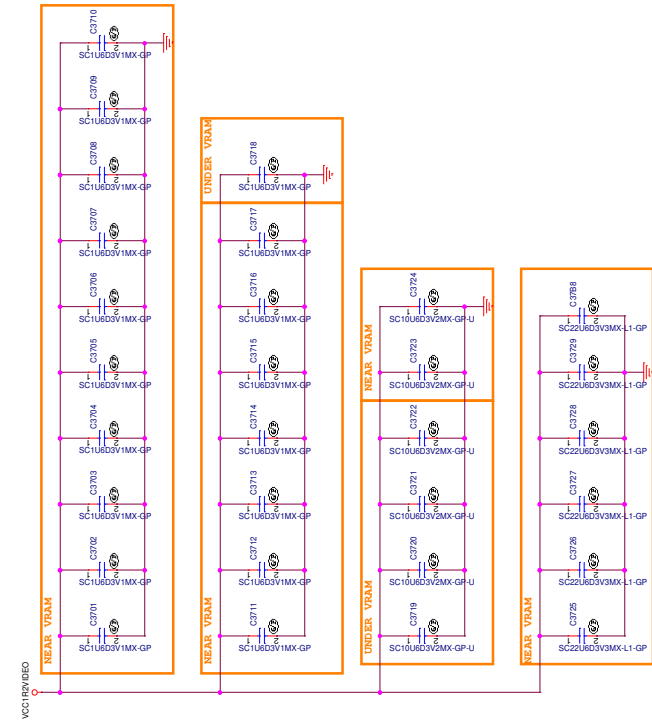




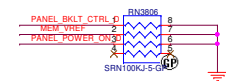
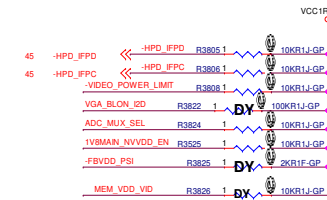
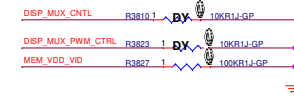
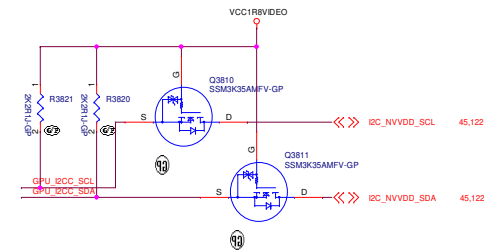
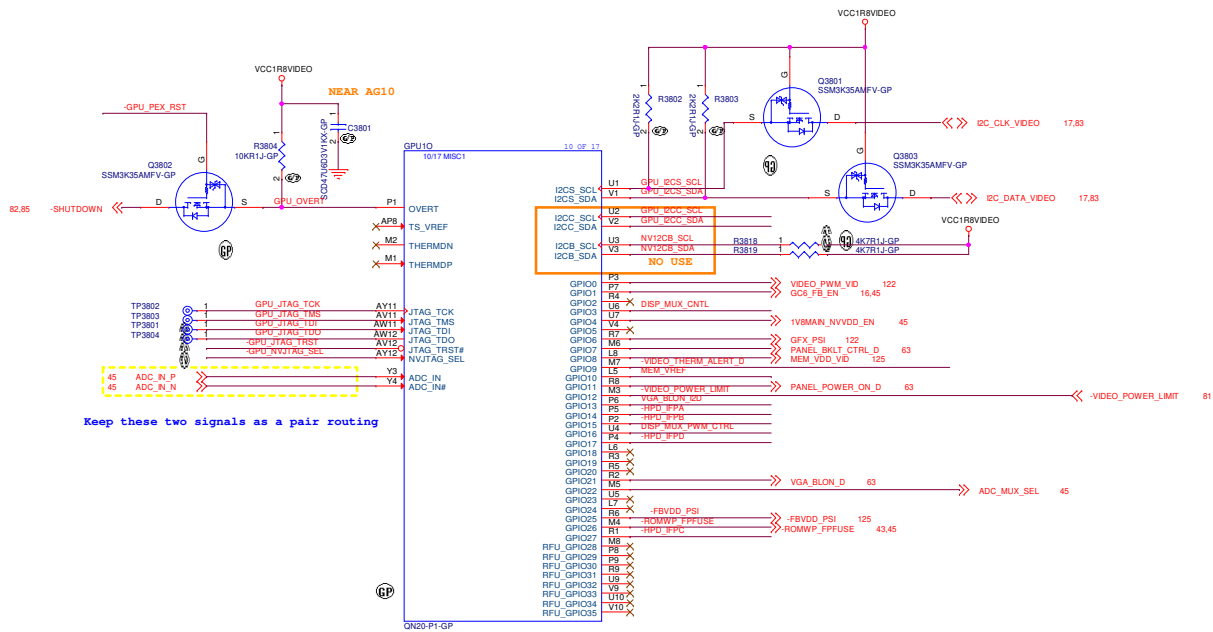








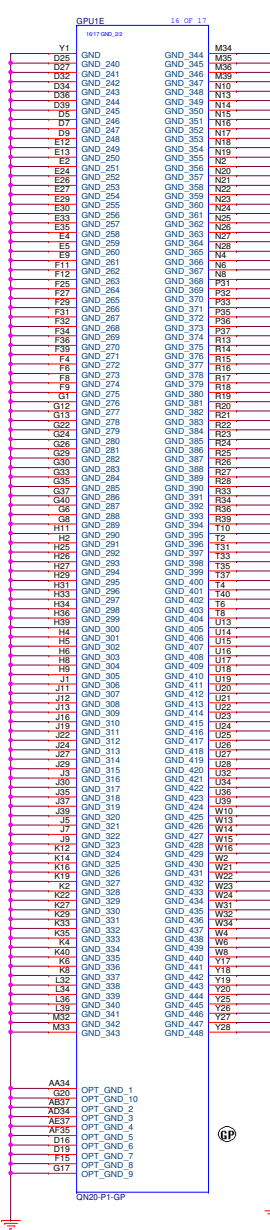
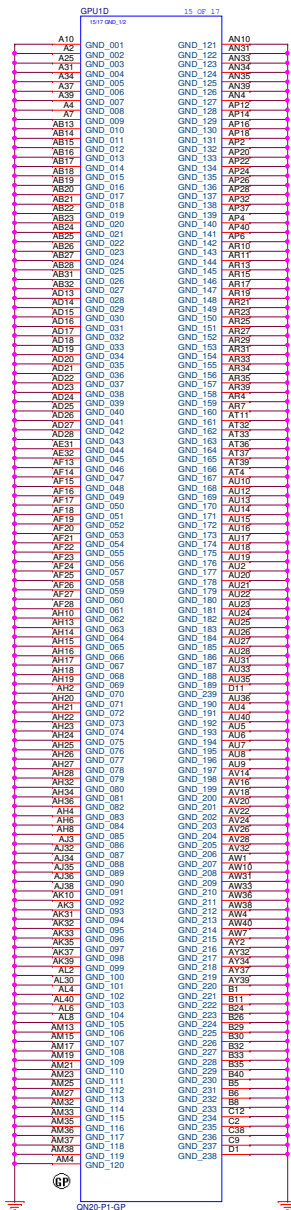












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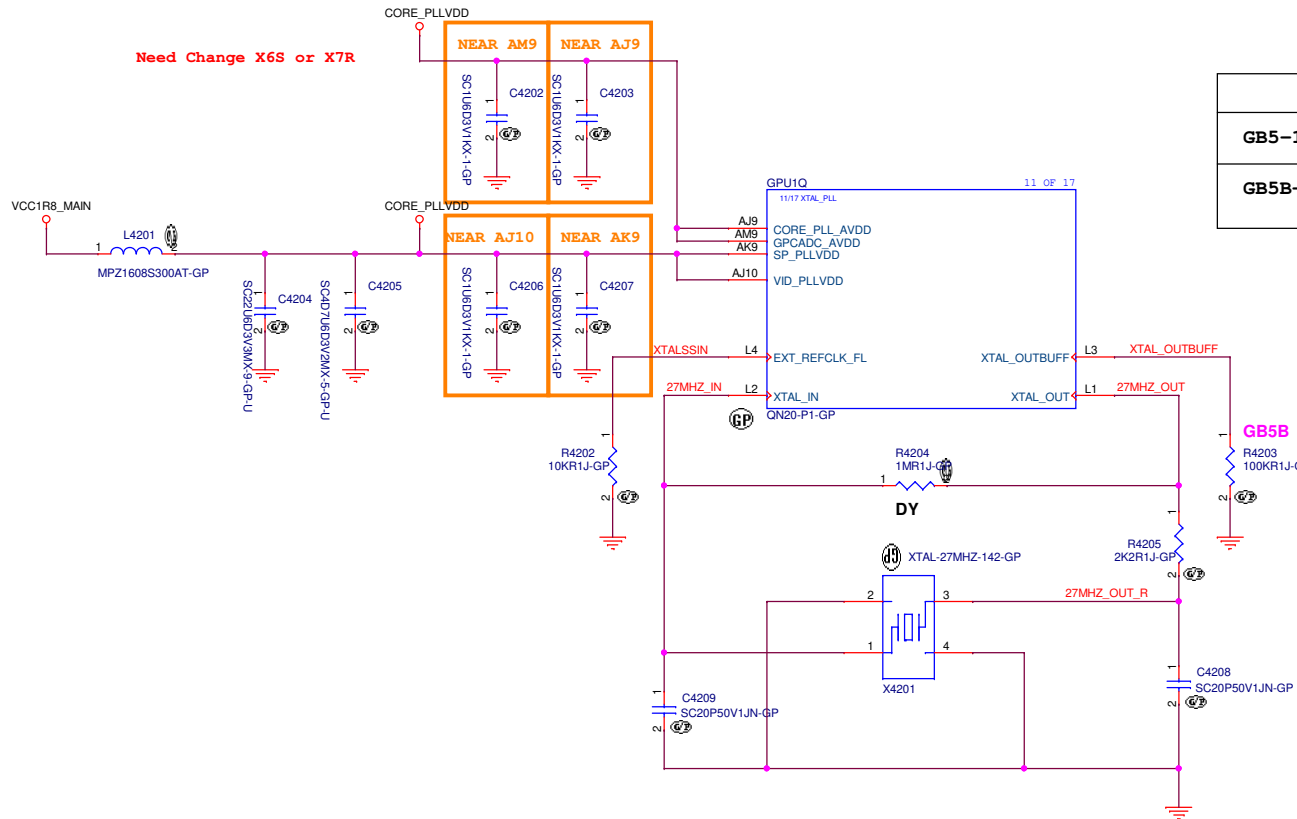
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File N20P GND			
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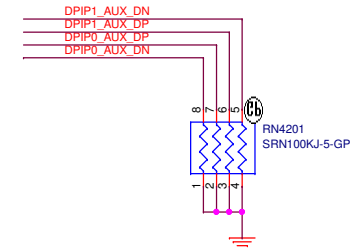




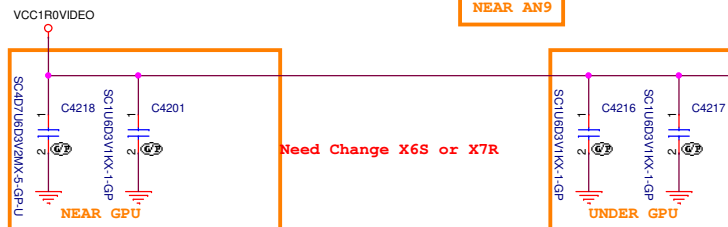
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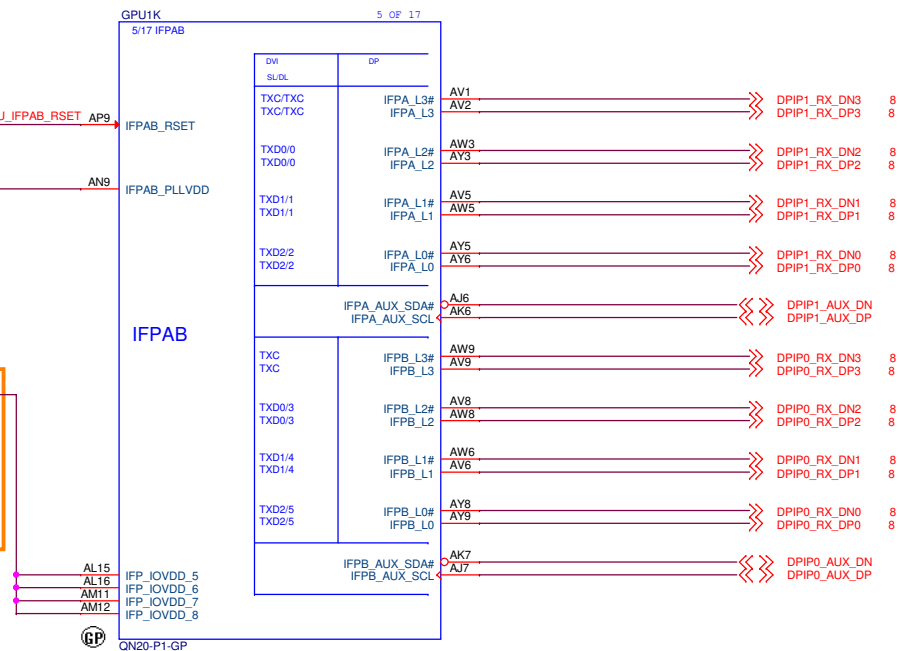
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<b>GB5-128</b>	<b>ASM</b>
<b>GB5B-128</b>	<b>N0-ASM</b>



2 port x 305mA



Need Change X6S or X7R



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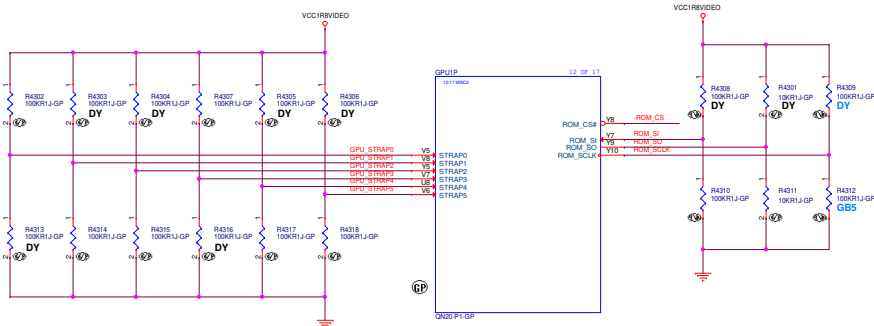
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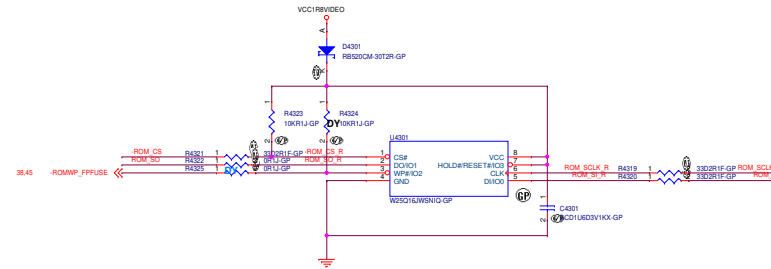
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	ROM_SO	ROM_SI	ROM_SCLK	R4325	R4324	U4301
GB5-128 (QN20-P1)	L	L	L	No-ASM	ASM	8Mb-W25Q80EW 8Mb-MX25U8033EM1I-12G
GB5B-128 (QN20-P3)	L	L	H	ASM	No-ASM	16Mb-W25Q16JW



Strap table				Strap0		Strap1		Strap2		VRAM1 VRAM2 VRAM3 VRAM4			
				STRAP0_H@	STRAP0_L@	STRAP1_H@	STRAP1_L@	STRAP2_H@	STRAP2_L@				
GPU	Vendor	DIE Rev	Strap	R4302	R4313	R4303	R4314	R4304	R4315				
QN20-P3_8G	Samsung	C	0x0	NO ASM	ASM	NO ASM	ASM	NO ASM	ASM	ASM	ASM	ASM	ASM
	Hynix	A	0x2	NO ASM	ASM	ASM	NO ASM	NO ASM	ASM	ASM	ASM	ASM	ASM
QN20-P1_8G	Samsung	C	0x0	NO ASM	ASM	NO ASM	ASM	NO ASM	ASM	ASM	ASM	ASM	ASM
	Micron	A	0x1	ASM	NO ASM	NO ASM	ASM	NO ASM	ASM	ASM	ASM	ASM	ASM
GN20-P1_8G	Samsung	C	0x0	NO ASM	ASM	NO ASM	ASM	NO ASM	ASM	ASM	ASM	ASM	ASM
	Hynix	A	0x2	NO ASM	ASM	ASM	NO ASM	NO ASM	ASM	ASM	ASM	ASM	ASM
	Micron	A	0x1	ASM	NO ASM	NO ASM	ASM	NO ASM	ASM	ASM	ASM	ASM	ASM

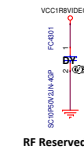


Table 5.3 RAMCFG

Strap Pins see Note			RAMCFG Setting Number	
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)	
L	L	L	0 (0x0000)	
L	L	H	1 (0x0001)	
L	H	L	2 (0x0002)	
L	H	H	3 (0x0003)	
H	L	L	4 (0x0004)	
H	L	H	5 (0x0005)	
H	H	L	6 (0x0006)	
H	H	H	7 (0x0007)	
L	L	M	8 (0x0008)	
L	M	L	9 (0x0009)	
L	M	H	10 (0x000A)	
L	H	M	11 (0x000B)	
M	L	L	12 (0x000C)	
M	L	H	13 (0x000D)	

Strap Pins see Note			RAMCFG Setting Number	
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)	
M	H	L	14 (0x000E)	
M	H	H	15 (0x000F)	
H	L	M	16 (0x0010)	
H	M	L	17 (0x0011)	
H	M	H	18 (0x0012)	
H	H	M	19 (0x0013)	
L	M	M	20 (0x0014)	
M	L	M	21 (0x0015)	
M	M	L	22 (0x0016)	
M	M	H	23 (0x0017)	
M	H	M	24 (0x0018)	
H	M	M	25 (0x0019)	
M	M	M	26 (0x001A)	

Table 12.5 SMB\_ALT\_ADDR, DEVID\_SEL, PCIE\_CFG, VGA\_DEVICE

Strap Pins See Note			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0
L	L	H	0	0	0	1
L	H	L	0	0	1	0
L	H	H	0	0	1	1
H	L	L	0	1	0	0
H	L	H	0	1	0	1
H	H	L	0	1	1	0
H	H	H	0	1	1	1
L	L	M	1	0	0	0
L	M	L	1	0	0	1
M	M	H	1	0	1	0

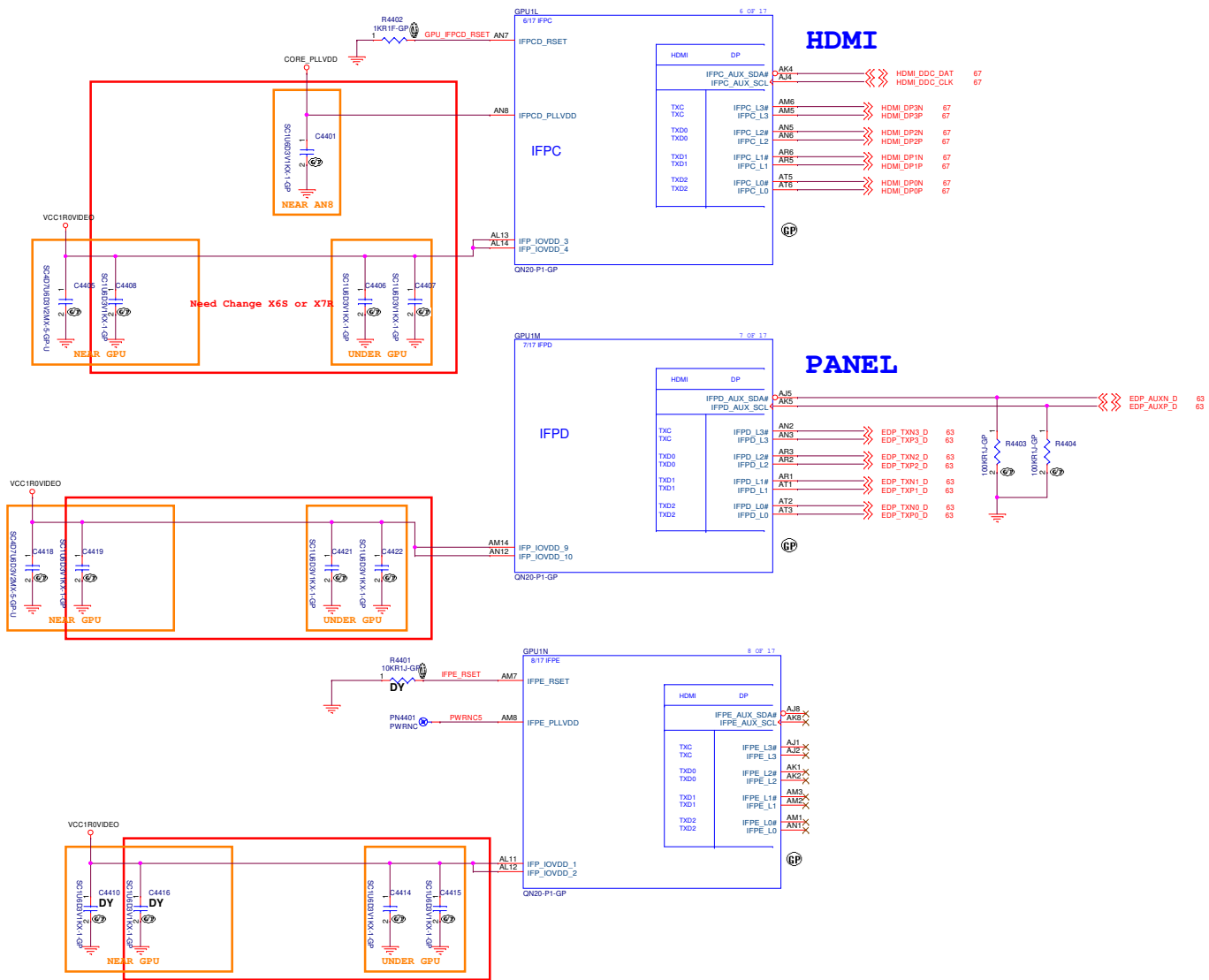
Strap Pins See Note			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	H	M	1	0	1	1
M	L	L	1	1	0	0
M	L	H	1	1	0	1
M	H	L	1	1	1	0
M	H	H	1	1	1	1
H	L	M				
H	M	L				
H	M	H				
H	H	M				
M	M	L				
M	M	H				
M	H	M				
M	M	M				

## 12.2.2.4 Assorted Configuration Straps

The following configurable characteristics of the graphics circuit share three physical strap pins:

- **SMB\_ALT\_ADDR Enable:** This strap function allows an alternate SMBus address to be configured, so that graphics circuits with multiple GPUs can have separate SMBus connections for each GPU. In dual GPU configurations, use of the alternate address on one GPU (by setting this function to '1') avoids conflicts between the two GPUs on an SMBus port. The "SMB\_ALT\_ADDR disabled" setting ('0') is correct for single-GPU graphics circuits.
- **DEVID\_SEL:** NVIDIA defines an original and a re-brand Device ID on a per-GPU basis. This Device ID Select strap function allows selection between the original PCIe Device ID defined for the GPU (via a function setting of '0'), and the alternate "re-brand" Device ID defined for the GPU (via a function setting of '1').
- **PCIE\_CFG:** This function sets electrical characteristics of PCIe lanes, in particular signal amplitude (swing). A setting of '0' selects normal (full) signal swing. N188 graphics circuits should strap for this setting. (A setting of '1' designates reduced signal amplitude, available if special concerns require. Consult NVIDIA for guidance.)
- **VGA\_DEVICE:** This strap function is used to report the graphics circuit either as a 3D device (class code 302, designated by a setting of '0' for this strap) or as a VGA device (class code 300, designated by a setting of '1') to the host system. The 3D Device (class code 302, strap='0') setting is correct for most MS-Hybrid notebook GeForce graphics circuits (consult NVIDIA for details on proper bit setting for MS-Hybrid solutions).





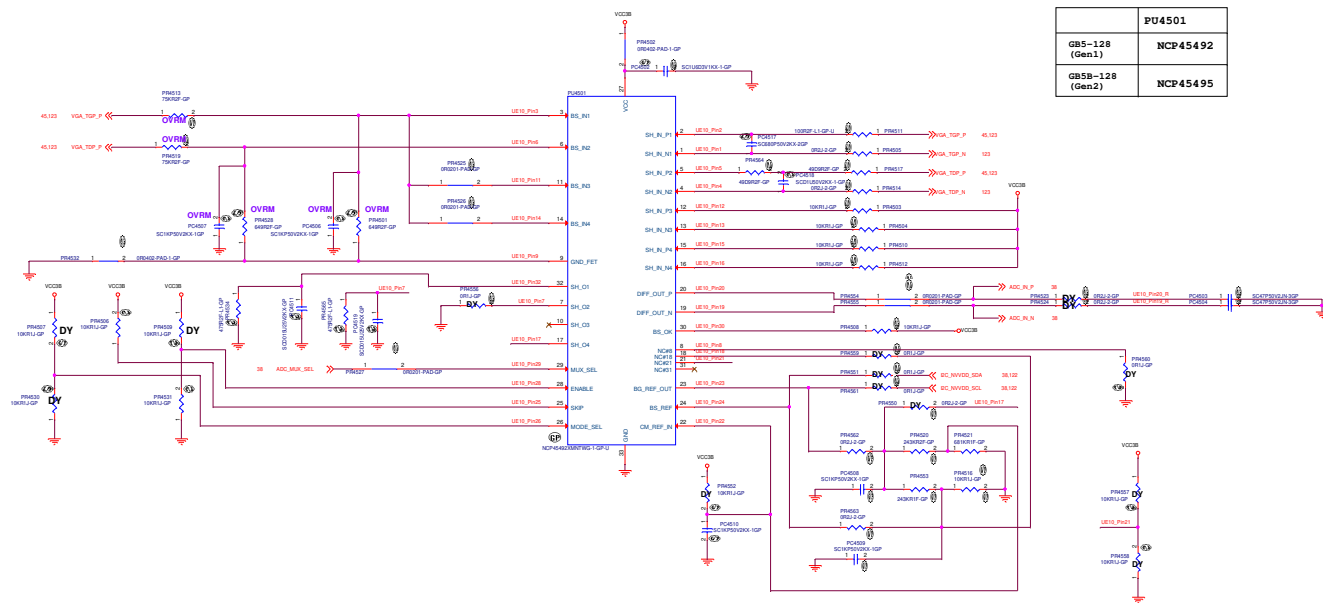
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PU4501	
GB5-128 (Gen1)	NCP45492
GB5B-128 (Gen2)	NCP45495

Please change the red character value for OVR-M Gen1/Gen2 BOM Option table

PR4513 (R22)		PR4501 (R23)	PC4506 (CA)	PR4519 (R27)	PR4508 (R26)	PC4597 (C6)
Gen1	75K ohm	649 ohm	1 nF	75K ohm	649 ohm	1 nF
Gen2	0 ohm	No-ASM	No-ASM	0 ohm	No-ASM	No-ASM

PR4511 (R1)		PR4505 (R2)	PC4517 (C1)	PR4564 (R3)	PR4517 (R4)	PR4514 (R5)	PC4508 (C2)
Gen1	100 ohm	0 ohm	680 pF	49.9 ohm	49.9 ohm	0 ohm	0.1 uF
Gen2	0 ohm	0 ohm	680 pF	49.9 ohm	49.9 ohm	0 ohm	0.1 uF

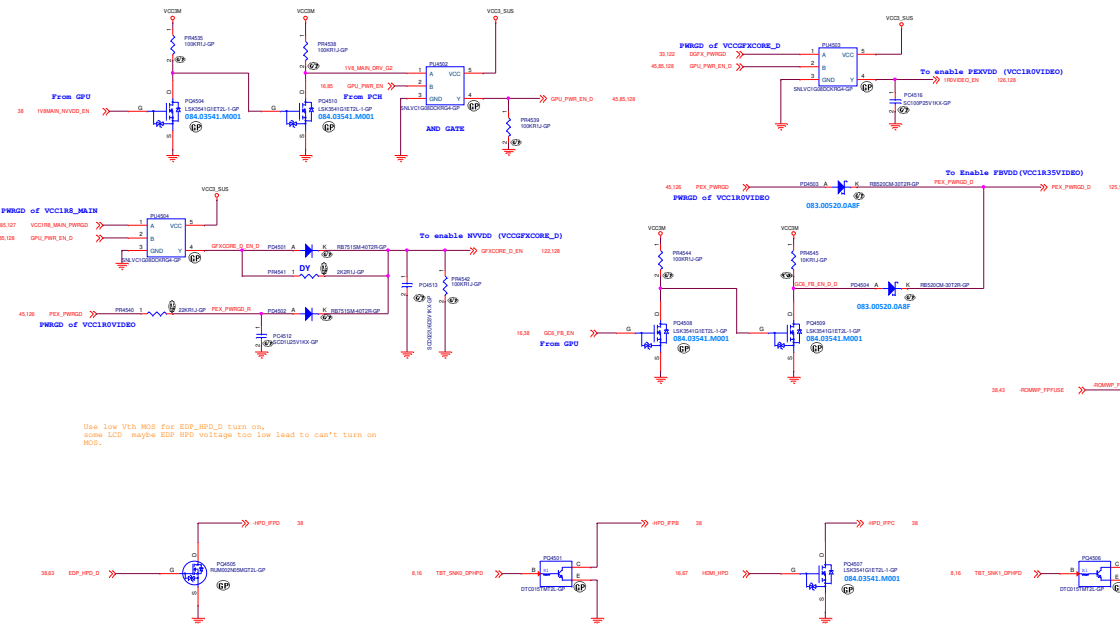
PR4534 (R21)		PC4513 (C10)	PR4505 (R25)	PC4509 (C11)	PR4508 (R26)	PR4508 (R20)	PC4508 (C8)	PR4503 (R17)	PR4502 (R12)	PR4502 (R13)
Gen1	475 ohm	15 nF	475 ohm	15 nF	No-ASM	No-ASM	1 nF	240K ohm	0 ohm	240K ohm
Gen2	No-ASM	No-ASM	No-ASM	No-ASM	0 ohm	No-ASM	1 nF	110K ohm	No-ASM	No-ASM

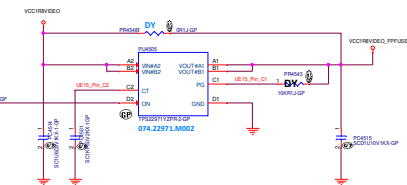
PR4560 (R7)		PR4509 (R8)	PR4516 (R18)	PC4509 (C7)	PR4560 (R15)	PR4507 (R9)	PR4508 (R10)
Gen1	No-ASM	No-ASM	10K ohm	1 nF	0 ohm	No-ASM	No-ASM
Gen2	0 ohm	0 ohm	10K ohm	1 nF	No-ASM	10K ohm	No-ASM

PR4561 (R11)		PR4501 (R14)	PR4516 (R18)	PR4502 (R10)	PC4510 (C3)
Gen1	No-ASM	681K ohm	No-ASM	No-ASM	1 nF
Gen2	0 ohm	10K ohm	0 ohm	No-ASM	No-ASM



PU4505, PR4547 PC4501, PC4514, PC4515		PR4548
GB5-128 (QN20P-Q1)	ASM	No-ASM
GB5B-128 (QN20P-Q3)	No-ASM	ASM





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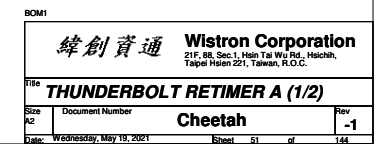
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# TBT Re-timer A Crystal

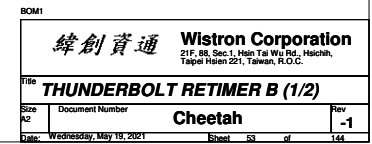








## TBT Re-timer B Crystal





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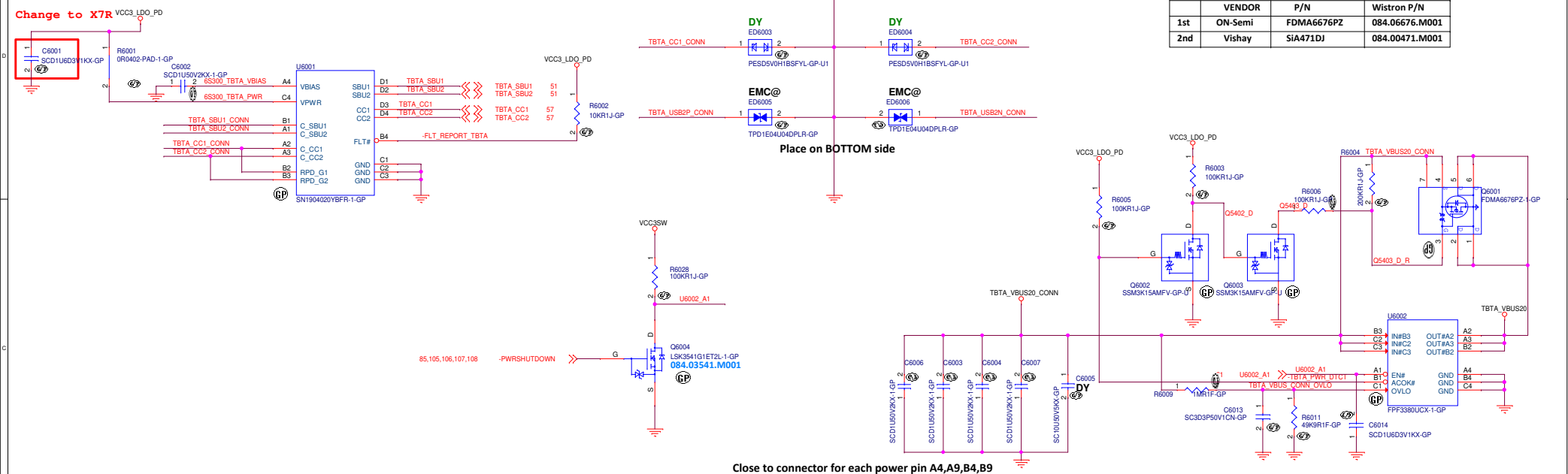
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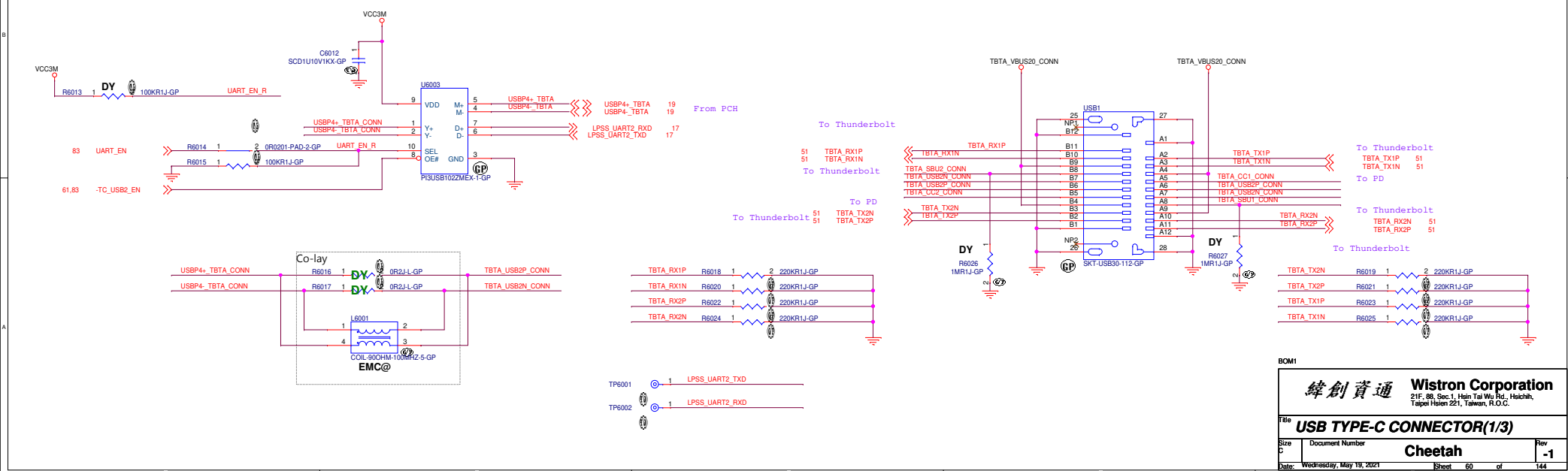
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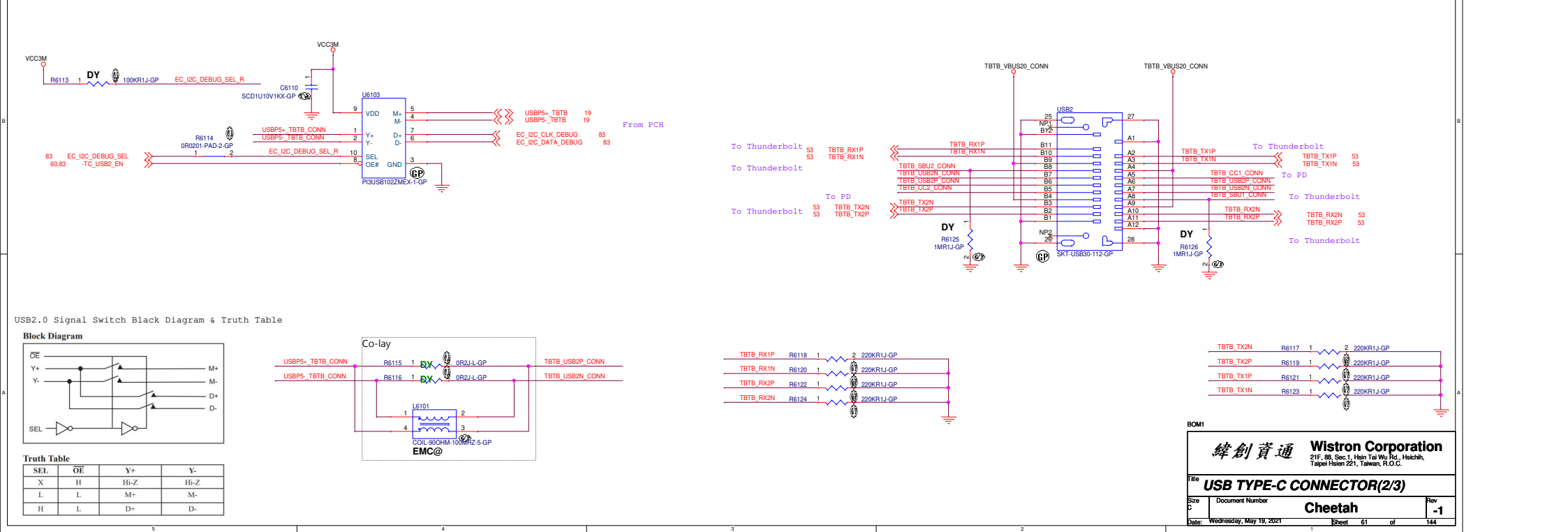
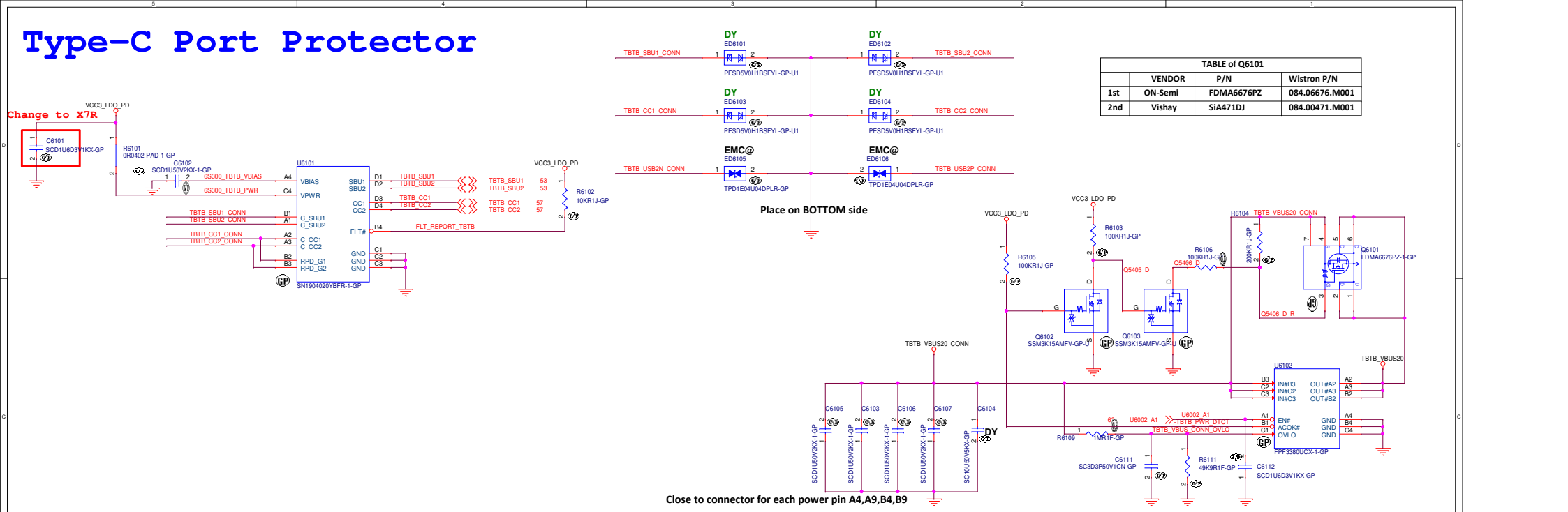
## Type-C Port Protector



## USB TYPE-C CONN 1







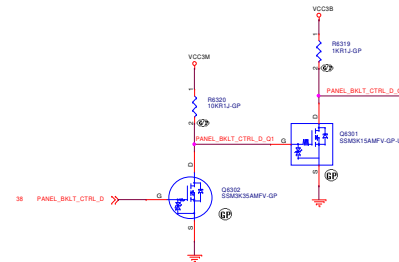
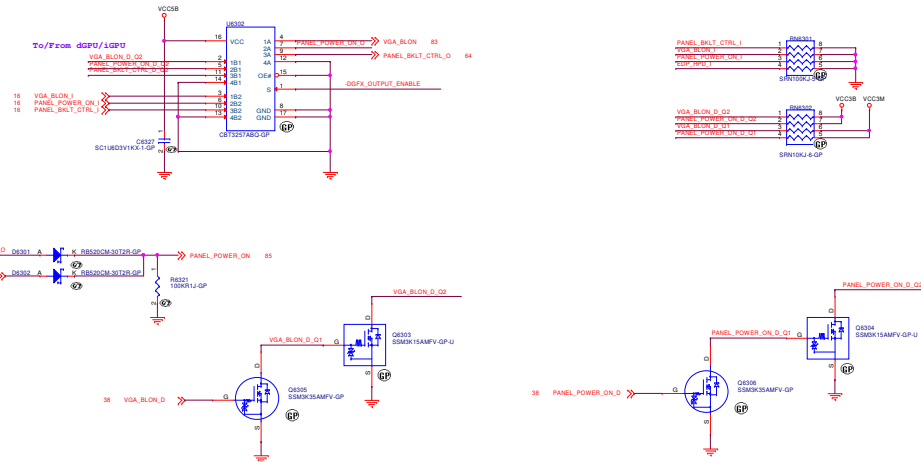


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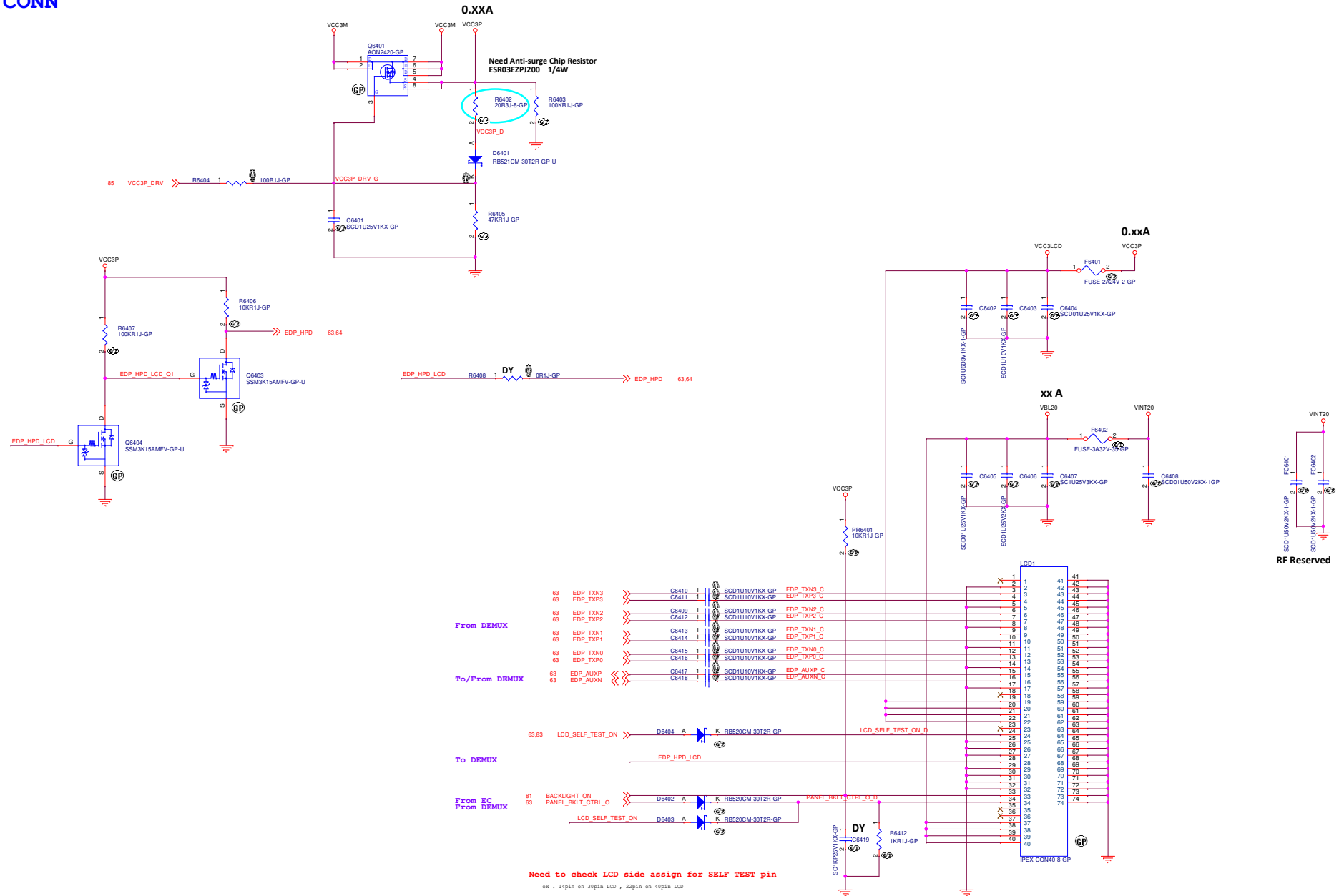
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**LCD CONN**





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Taipei Hsien 221, Taiwan, R.O.C.

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Size  
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Document Number

**Cheetah**

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**-1**

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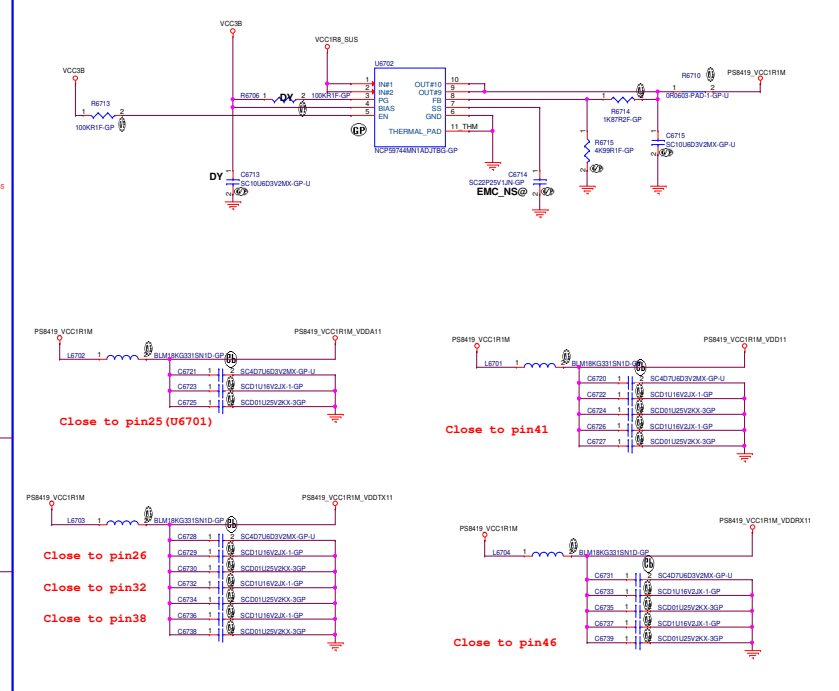


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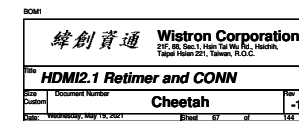
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**PS8419 PWR**



## HDMI 2.1 CONN





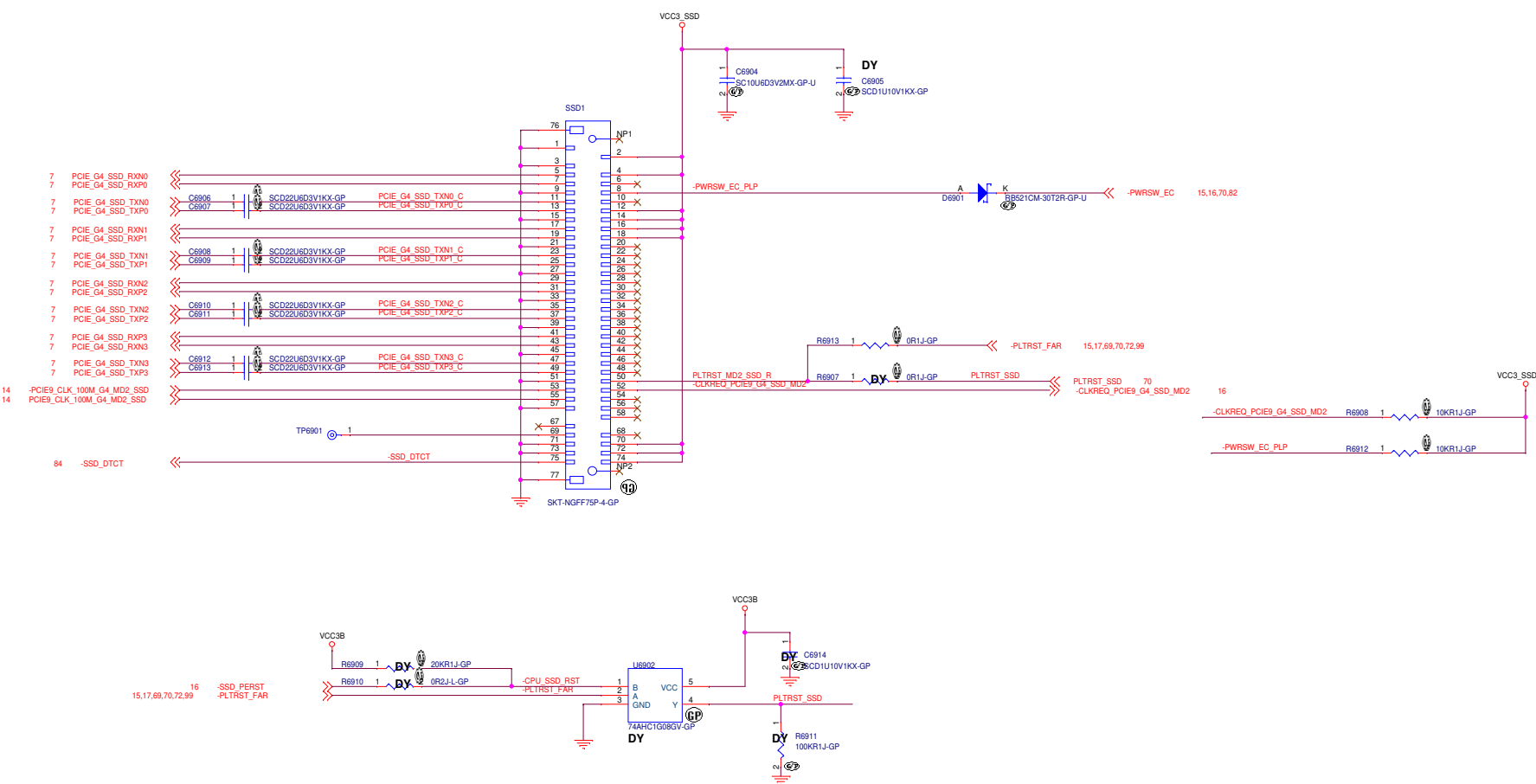
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M.2 SSD





# M.2 SSD

## M.2 SSD slot 2 Type-M 2280

### M.2 SSD2 L3

18 PCIE17L3\_MD2\_SSD2\_RXN << C7001 1 SCD22U6D3V1KX-GP PCIE17L3\_MD2\_SSD2\_TXN\_C  
18 PCIE17L3\_MD2\_SSD2\_TXN >> C7002 1 SCD22U6D3V1KX-GP PCIE17L3\_MD2\_SSD2\_TXP\_C

### M.2 SSD2 L2

18 PCIE17L2\_MD2\_SSD2\_RXN << C7003 1 SCD22U6D3V1KX-GP PCIE17L2\_MD2\_SSD2\_TXN\_C  
18 PCIE17L2\_MD2\_SSD2\_TXN >> C7004 1 SCD22U6D3V1KX-GP PCIE17L2\_MD2\_SSD2\_TXP\_C

### M.2 SSD2 L1

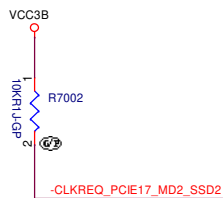
18 PCIE17L1\_MD2\_SSD2\_RXN << C7005 1 SCD22U6D3V1KX-GP PCIE17L1\_MD2\_SSD2\_TXN\_C  
18 PCIE17L1\_MD2\_SSD2\_TXN >> C7006 1 SCD22U6D3V1KX-GP PCIE17L1\_MD2\_SSD2\_TXP\_C

### M.2 SSD2 L0

18 PCIE17L0\_SATA4\_MD2\_SSD2\_RXP << C7007 1 SCD22U6D3V1KX-GP PCIE17L0\_SATA4\_MD2\_SSD2\_TXN\_C  
18 PCIE17L0\_SATA4\_MD2\_SSD2\_TXN >> C7008 1 SCD22U6D3V1KX-GP PCIE17L0\_SATA4\_MD2\_SSD2\_TXP\_C

14 -PCIE17\_CLK\_100M\_MD2\_SSD2  
14 PCIE17\_CLK\_100M\_MD2\_SSD2

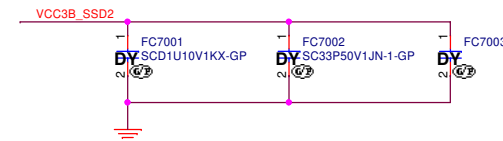
To EC



16 PCIE\_DETECT\_SSD2 <<  
84 -SSD2\_DTCT <<

TABLE

PCIE_DETECT_SSD2	Device
LOW	SATA SSD
High	PCIe SSD

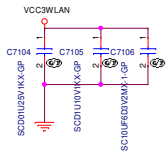
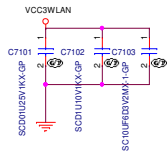
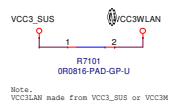


RF Reserved

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File M.2 PCIe GEN3 SSD Slot			
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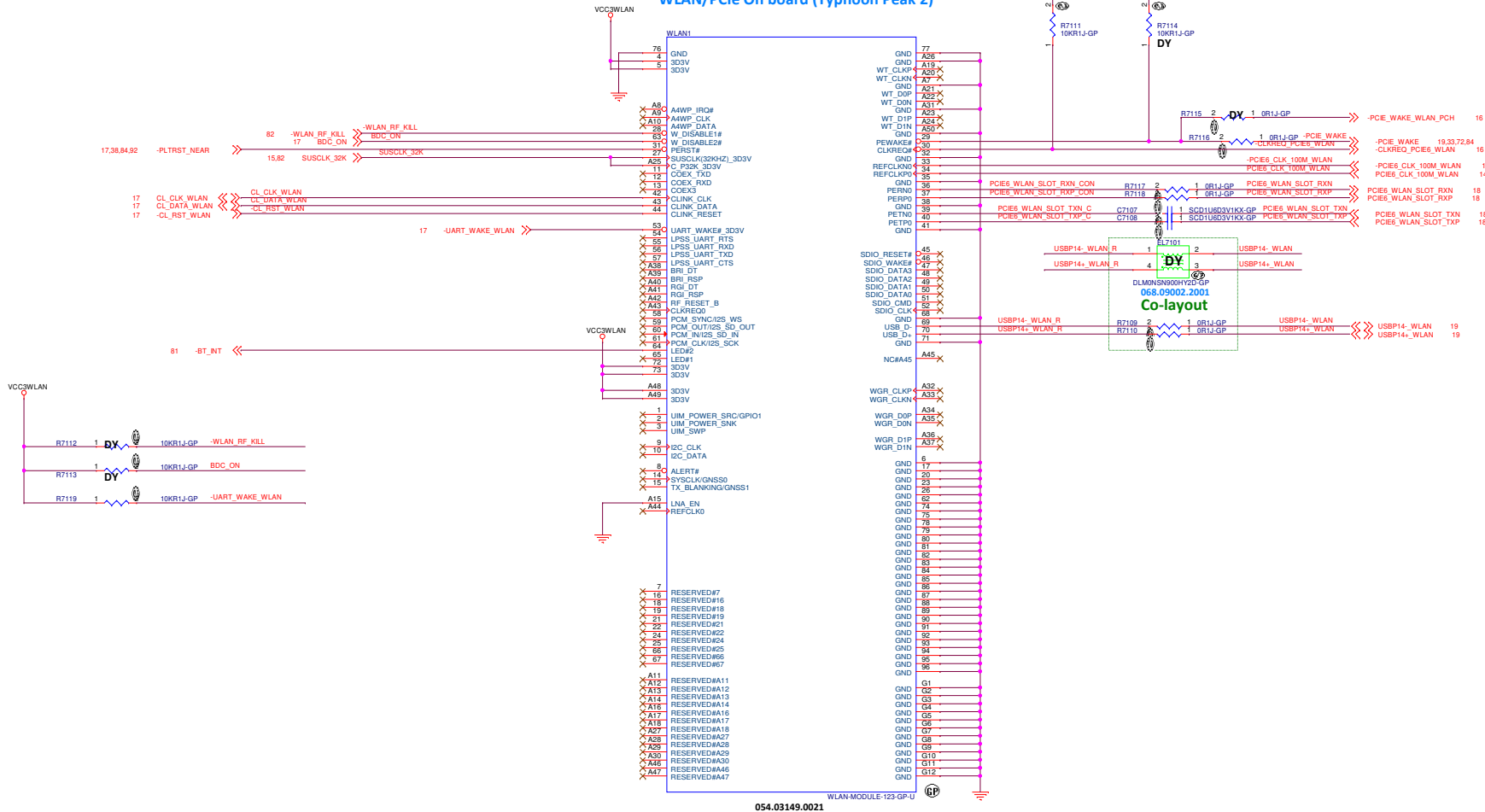




NEAR Pin4 Pin5

NEAR Pin72 Pin73

WLAN/PCIe On board (Typhoon Peak 2)





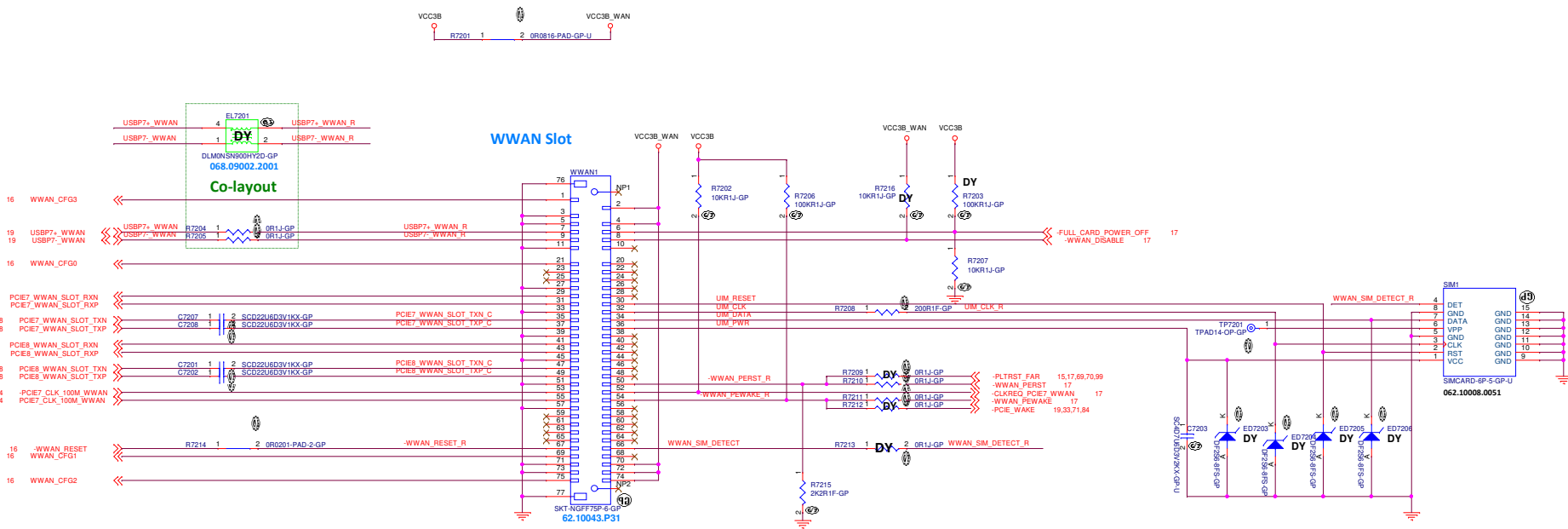
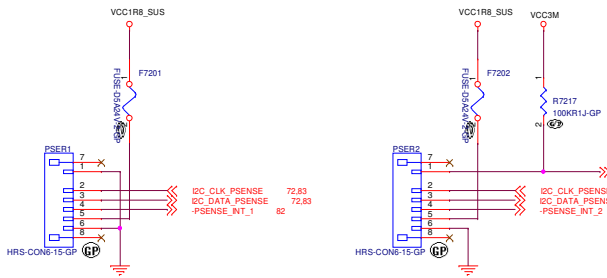


TABLE:

State #	Module Configuration Decodes				Module Type & Main Host Interface	Port Configuration
	CONFIG_0 (Pin 21)	CONFIG_3 (Pin 1)	CONFIG_2 (Pin 75)	CONFIG_1 (Pin 69)		
0	GND	GND	GND	GND	SSD - SATA	N/A
1	GND	GND	GND	NC	SSD - PCIe	N/A
2	GND	GND	NC	GND	WWAN - PCIe	0
3	GND	GND	NC	NC	WWAN - PCIe	1
4	GND	NC	GND	GND	WWAN - PCIe, USB 3.1 Gen1	0
5	GND	NC	GND	NC	WWAN - PCIe, USB 3.1 Gen1	1
6	GND	NC	NC	GND	WWAN - PCIe, USB 3.1 Gen1	2
7	GND	NC	NC	NC	WWAN - PCIe, USB 3.1 Gen1	3
8	NC	GND	GND	GND	WWAN - SSIC	0
9	NC	NC	GND	NC	WWAN - SSIC	1
10	NC	GND	NC	GND	WWAN - SSIC	2
11	NC	GND	NC	NC	WWAN - SSIC	3
12	NC	NC	GND	GND	WWAN - PCIe	2
13	NC	NC	GND	NC	WWAN - PCIe	3
14	NC	NC	NC	NC	WWAN - PCIe, USB 3.1 Gen1	Vendor Defined
15	NC	NC	NC	NC	No Module Present	N/A





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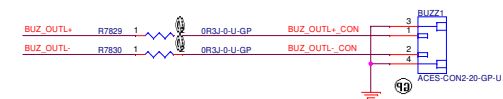
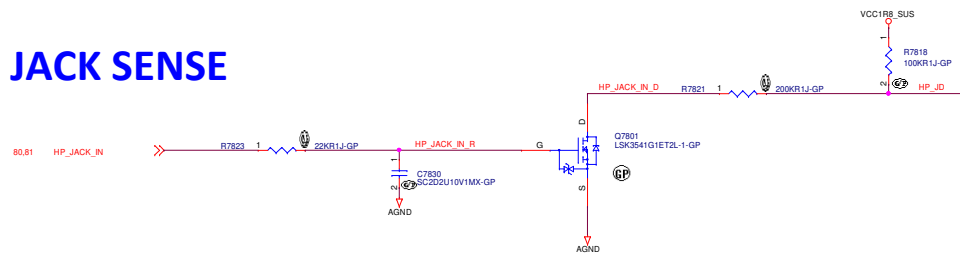
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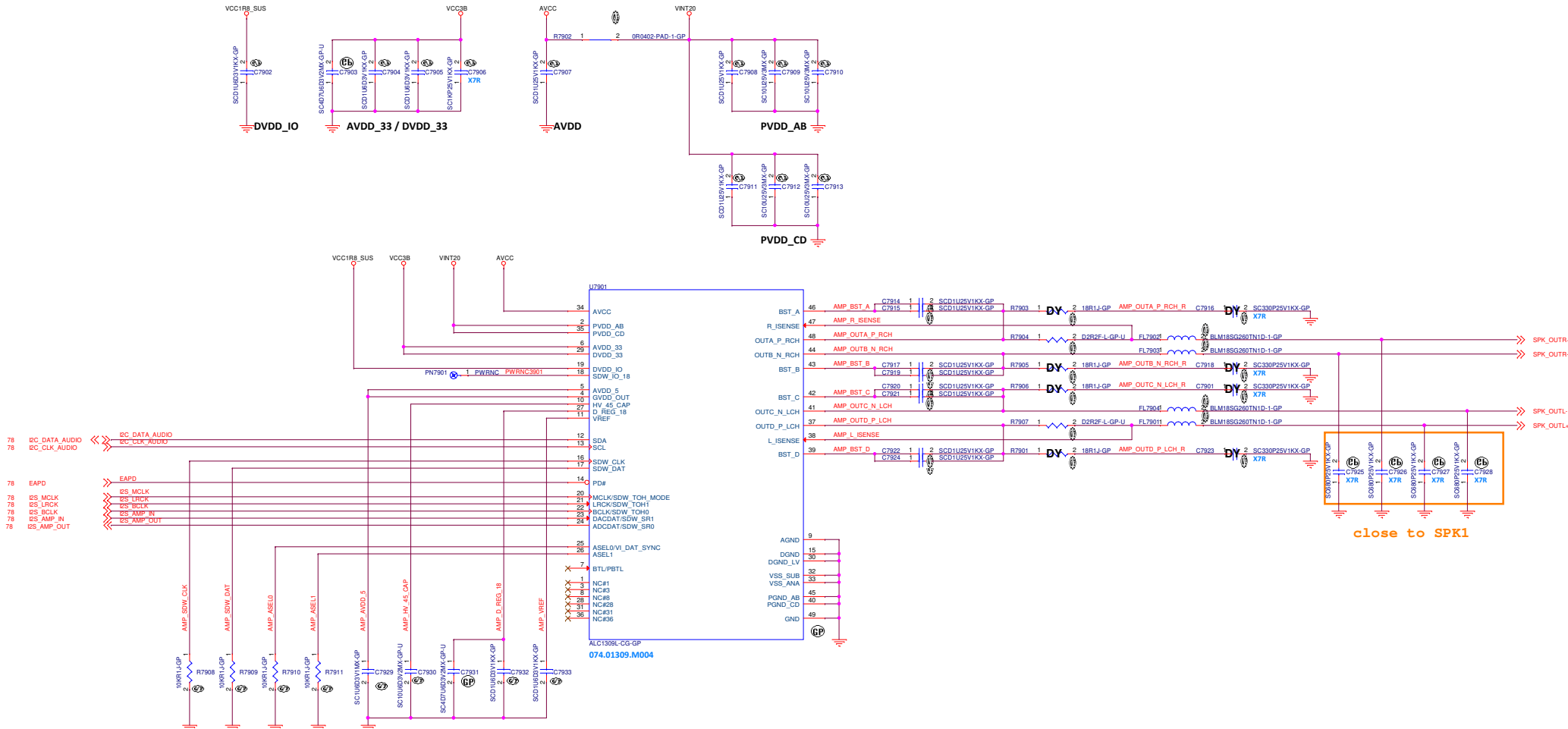


## AUDIO JACK SENSE



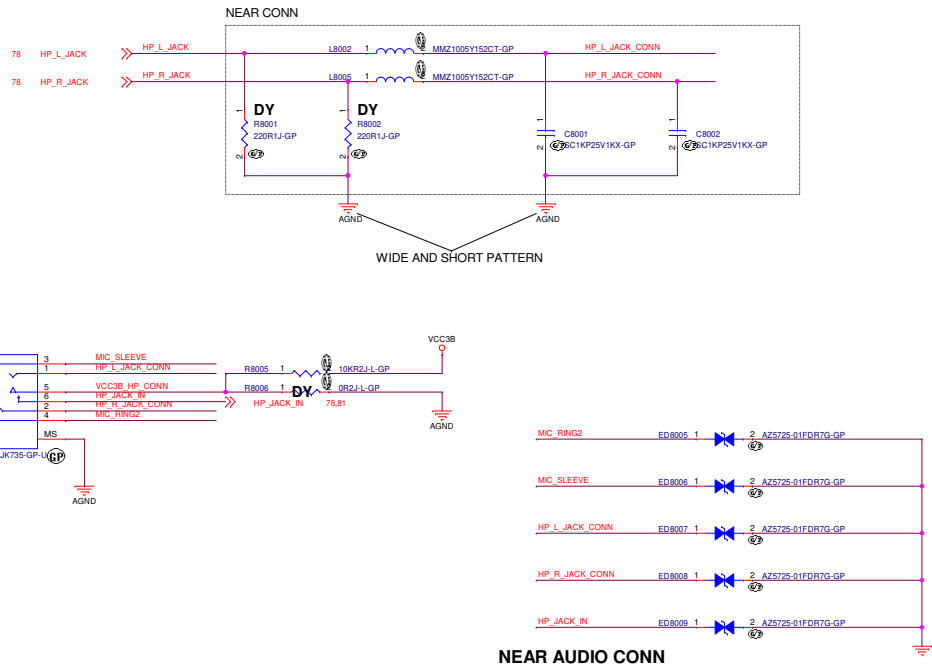


AUDIO SMART AMP (ALC1309)

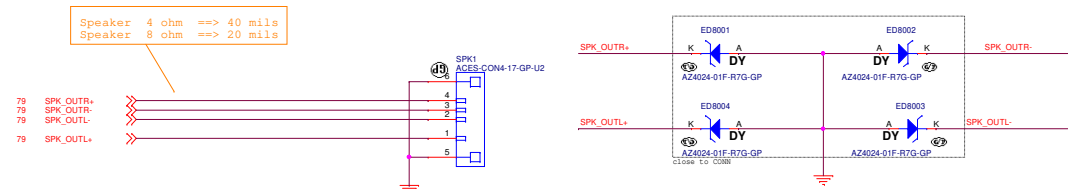




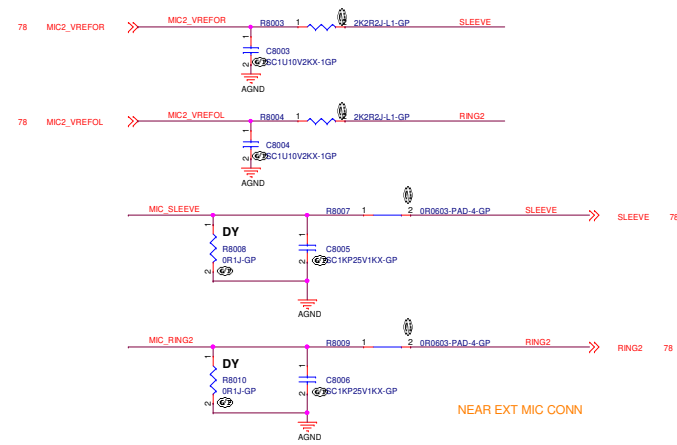
# AUDIO JACK



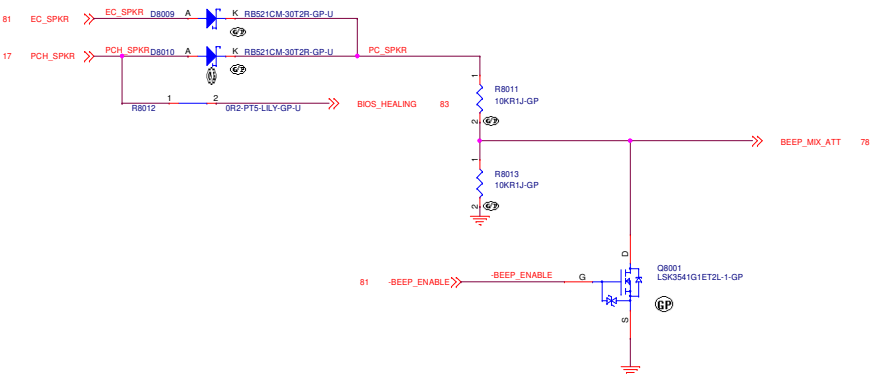
# SPEAKER



# HEAD PHONE

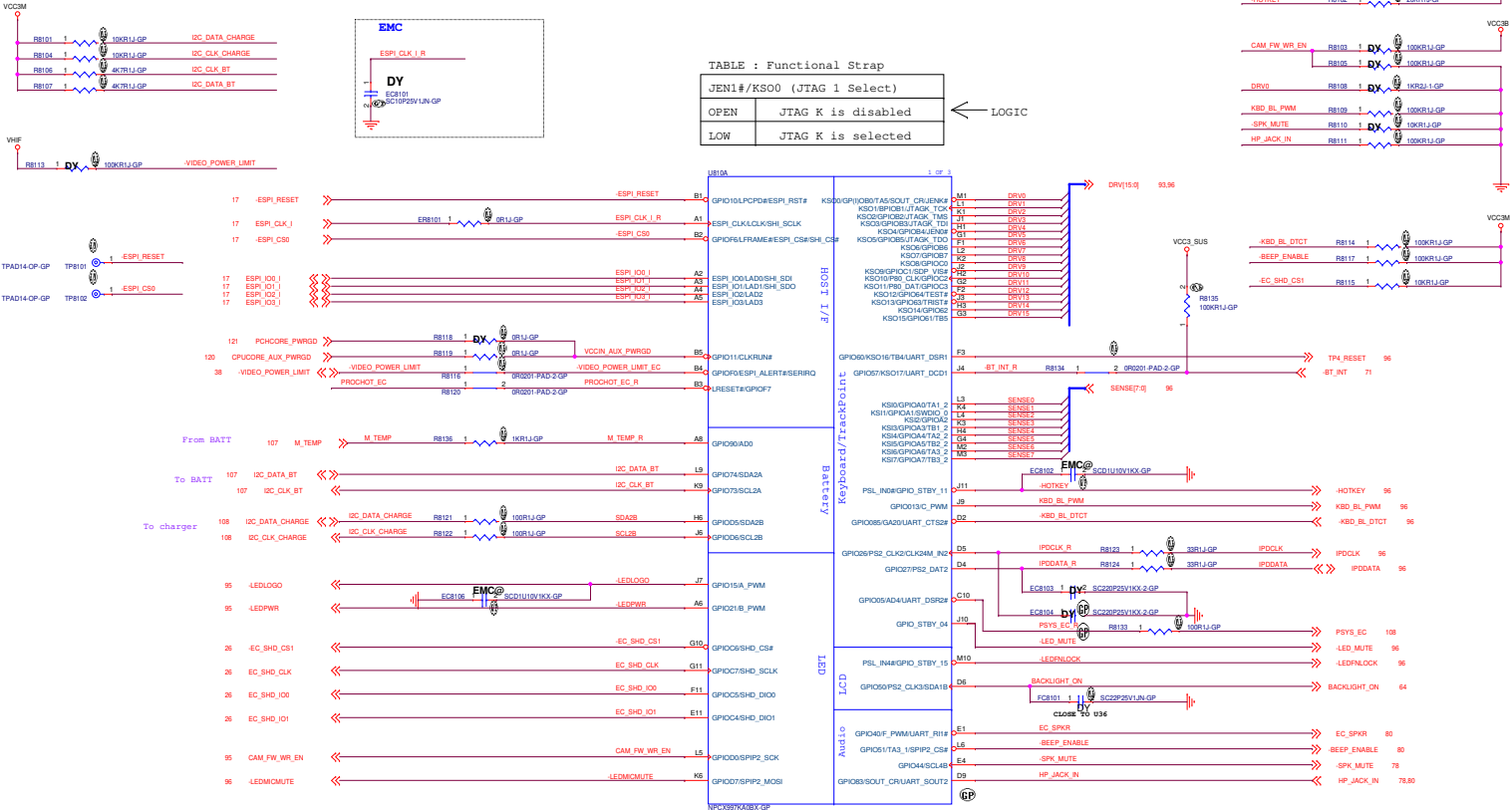


# PC BEEP



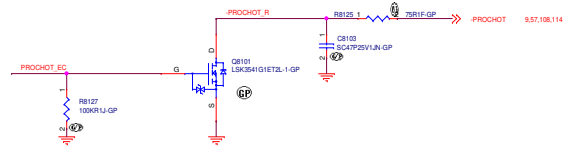


NPCX997 (1/3)

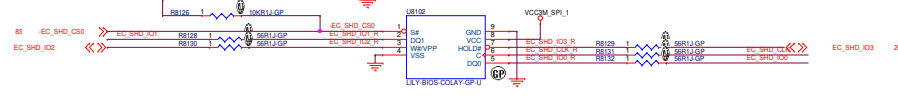


6. ELECTRICAL CHARACTERISTICS [T<sub>a</sub>=25°C] **OEC4 Vgs Threshold voltage**

PARAMETER	ITEM	CONDITION	MIN.	TYP.	MAX.
GATE THRESHOLD VOLTAGE	V <sub>GS(th)</sub>	V <sub>DS</sub> =3.0V / I <sub>D</sub> =100μA	0.8V	-	1.5V



EC SPI Flash

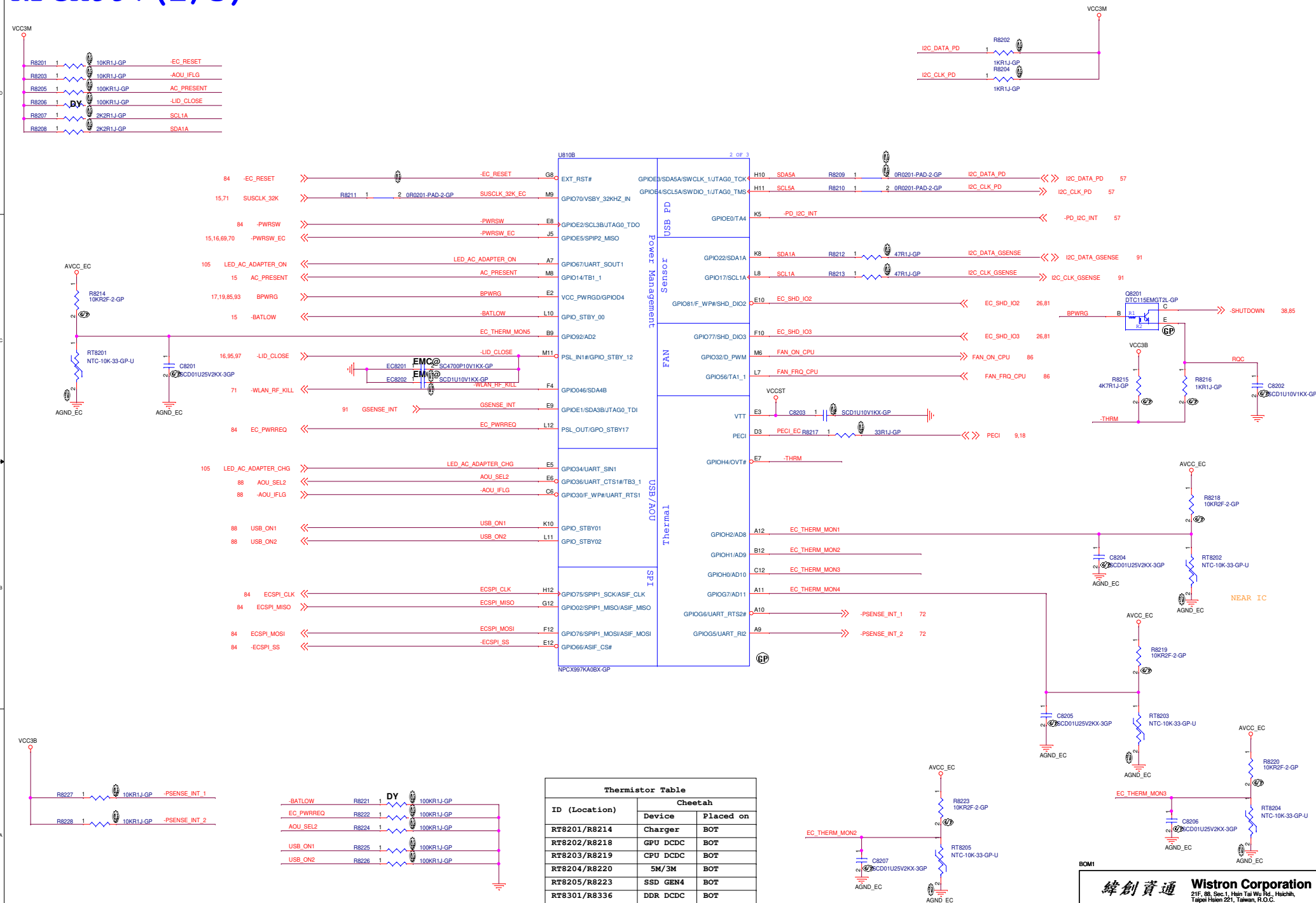


**TABLE U8102**  
32MB(256Mbit) 8x6mm WSON8 & SOP-8

Vender	Vender P/N	Wistron P/N
WINBOND	W25Q256VEIQ	072.25256.0N01
GIGADEVICE	GD25B256YIGR	072.25256.0B03
MXIC	MX25L25673GM21-08G	072.25673.0001



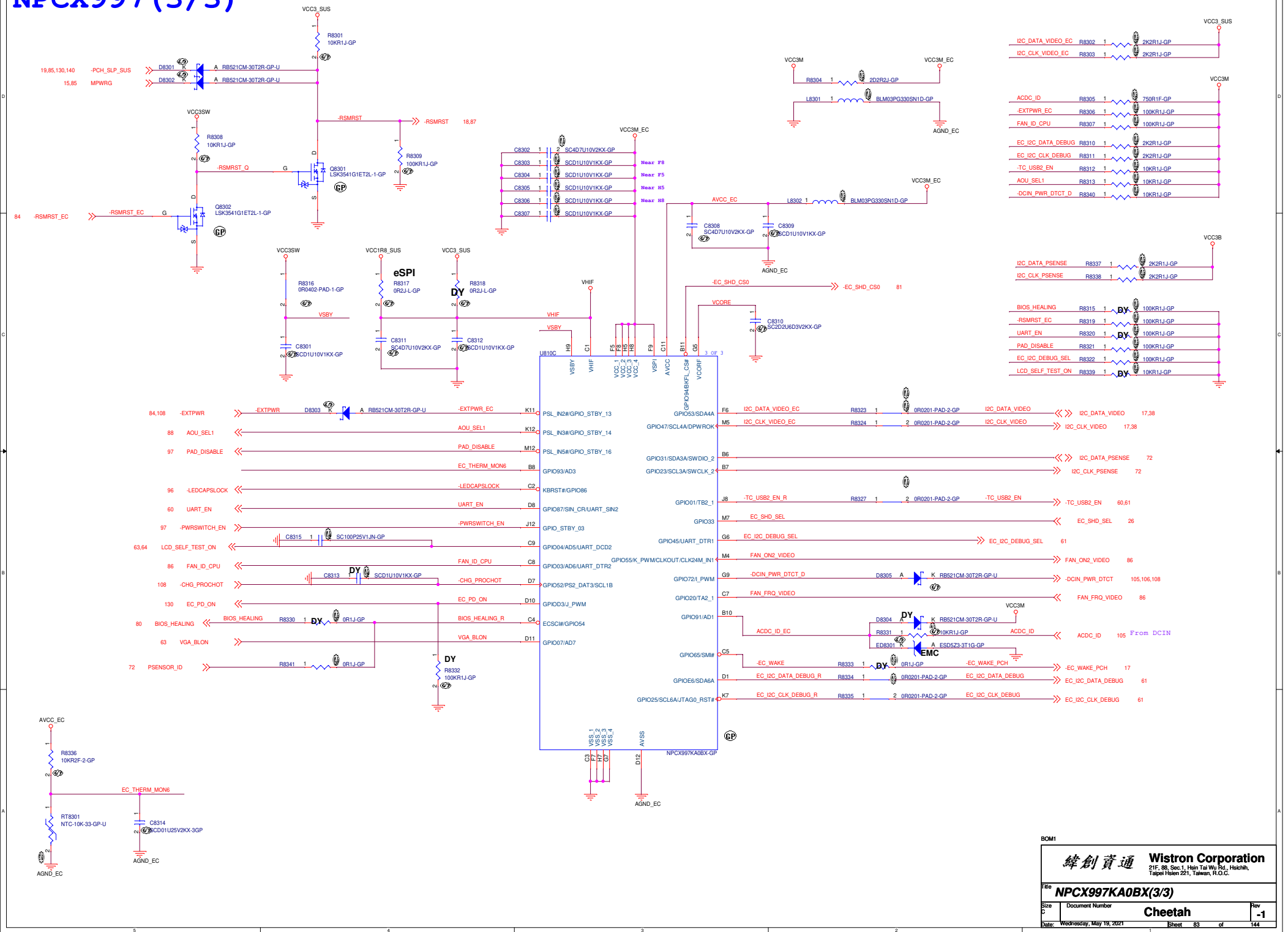
**NPCX997 (2/3)**



Thermistor Table		
ID (Location)	Cheetah	
	Device	Placed on
RT8201/R8214	Charger	BOT
RT8202/R8218	GPU DCDC	BOT
RT8203/R8219	CPU DCDC	BOT
RT8204/R8220	5M/3M	BOT
RT8205/R8223	SSD GEN4	BOT
RT8301/R8336	DDR DCDC	BOT

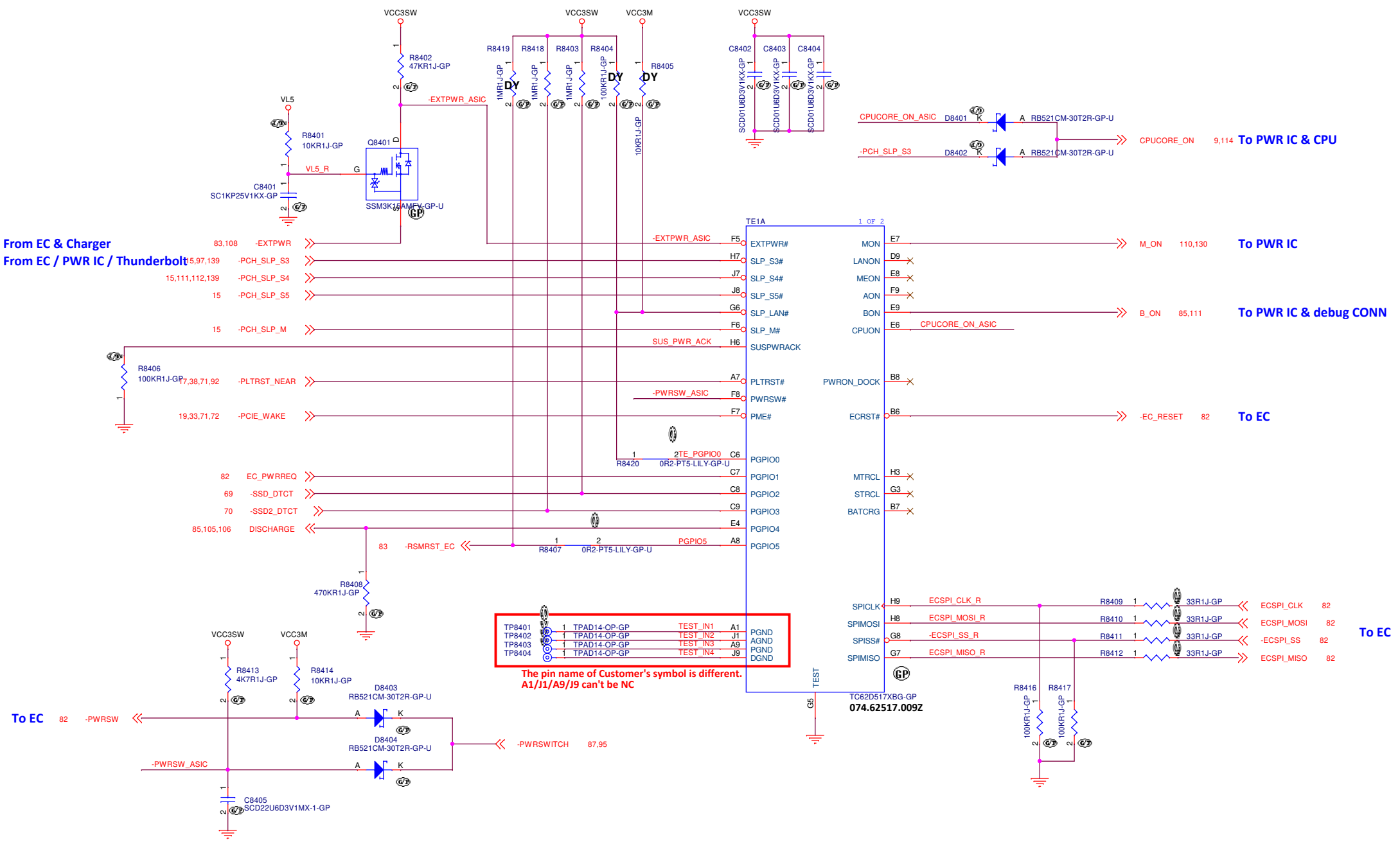


**NPCX997 (3/3)**



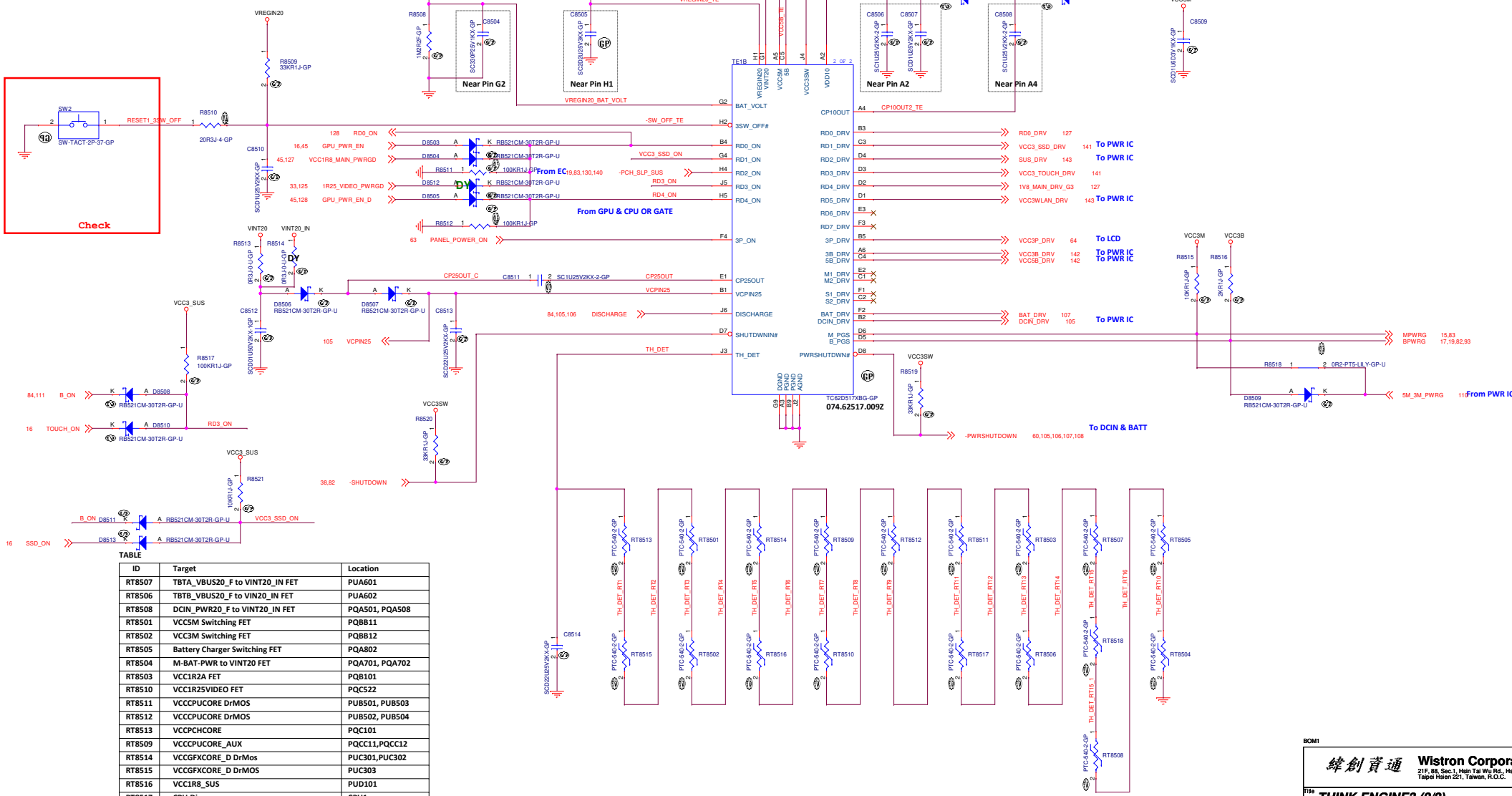


From EC & Charger  
From EC / PWR IC / Thunderbolt





	D8504	D8512	R8511
GB5-128 (QN20P-Q1)	ASM	No-ASM	100K
GB5B-128 (QN20P-Q3)	No-ASM	ASM	1M



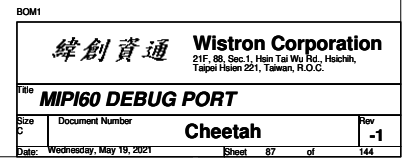
ID	Target	Location
RT8507	TBTA_VBUS20_F to VINT20_IN FET	PUA601
RT8506	TBTB_VBUS20_F to VIN20_IN FET	PUA602
RT8508	DCIN_PWR20_F to VINT20_IN FET	PQA501, PQA508
RT8501	VCC5M Switching FET	PQB811
RT8502	VCC3M Switching FET	PQB812
RT8505	Battery Charger Switching FET	PQA802
RT8504	M-BAT_PWR to VINT20 FET	PQA701, PQA702
RT8503	VCC1R2A FET	PQB101
RT8510	VCC1R2SVIDEO FET	PCQ522
RT8511	VCCCPUCORE DrMOS	PUB501, PUB503
RT8512	VCCCPUCORE DrMOS	PUB502, PUB504
RT8513	VCCPCHCORE	PQC101
RT8509	VCCPUCORE_AUX	PQC111, PQC112
RT8514	VCCGFXCORE_D DrMos	PUC301, PUC302
RT8515	VCCGFXCORE_D DrMOS	PUC303
RT8516	VCC1R8_SUS	PUD101
RT8517	CPU Die	CPU1
RT8518	VINT20_IN_A to VINT20 FET	PQA511, PQA510







**Need to be between CPU and EC**





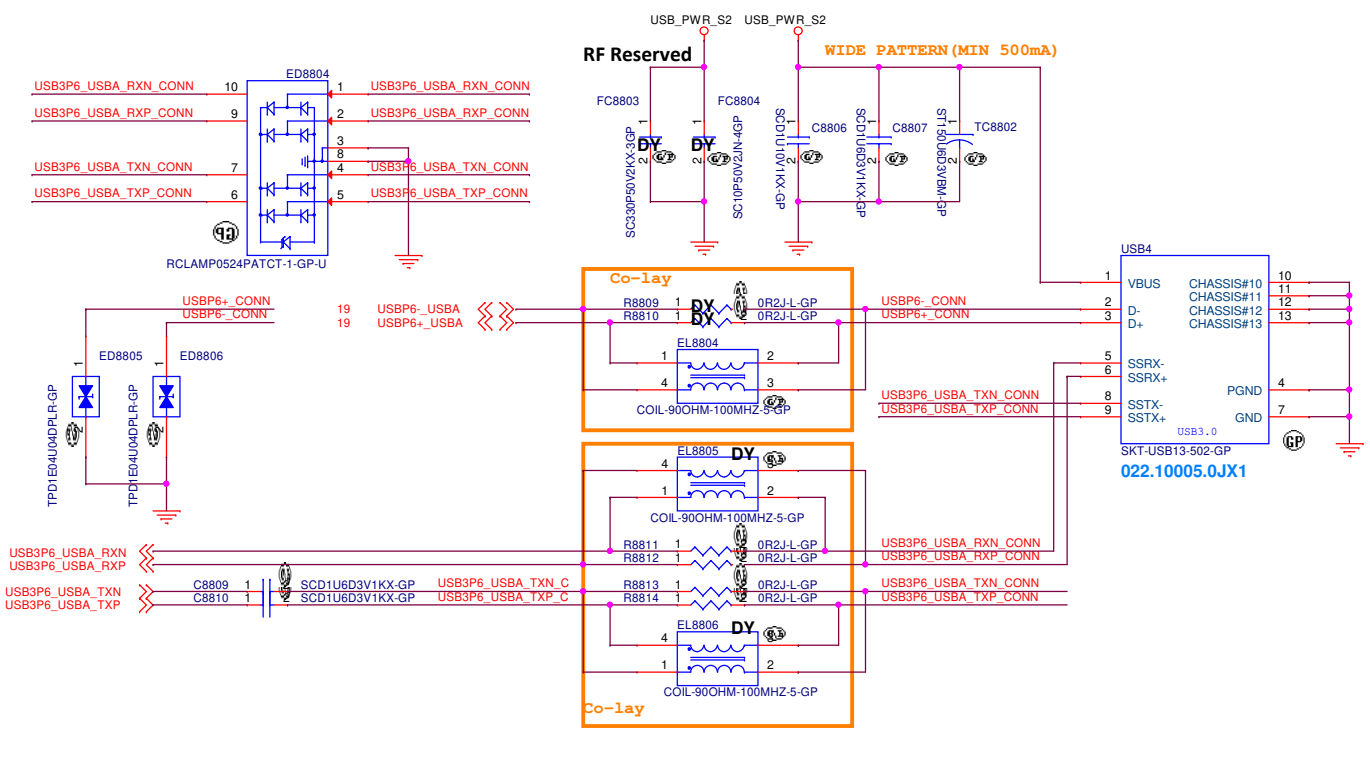
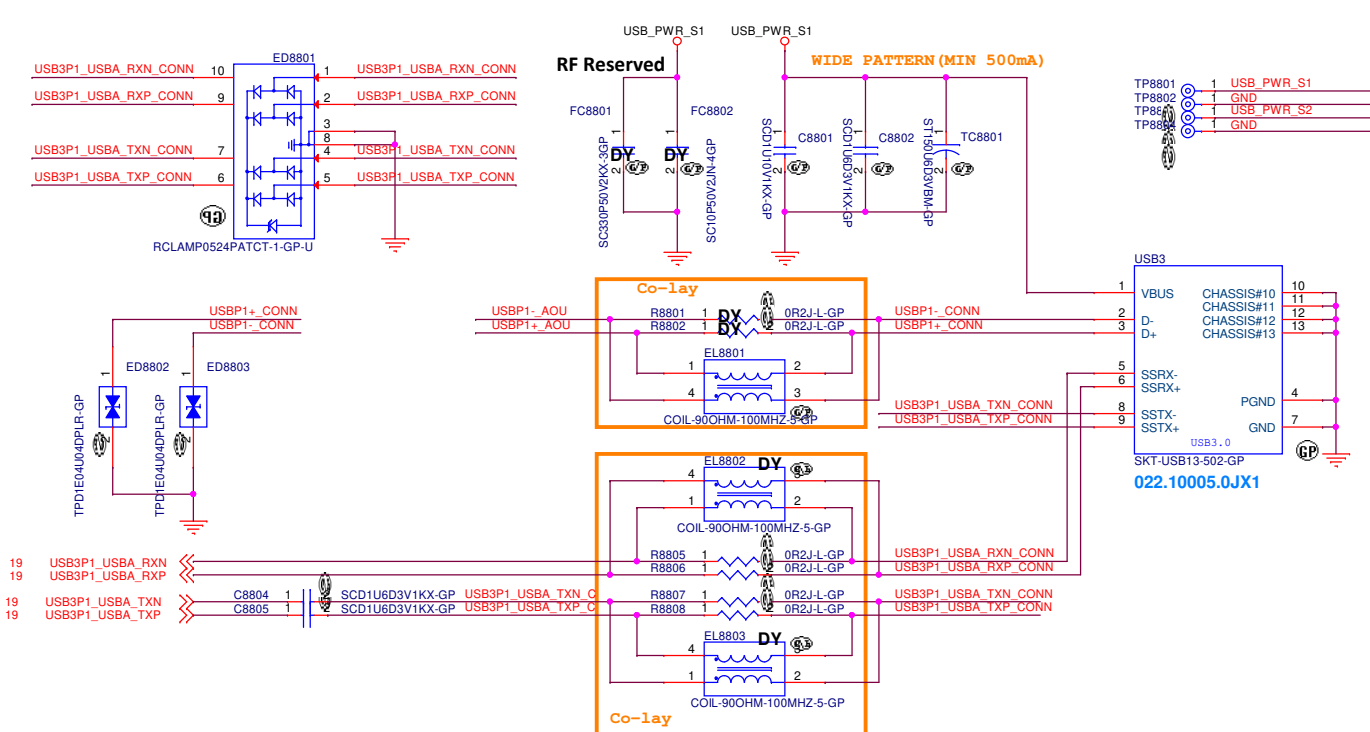
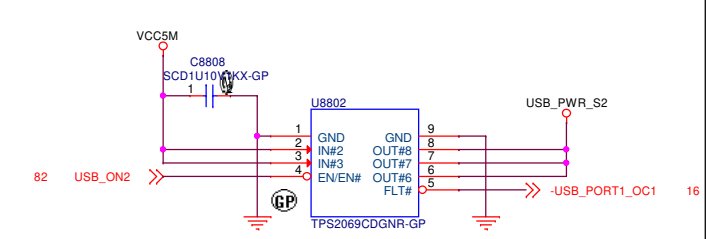
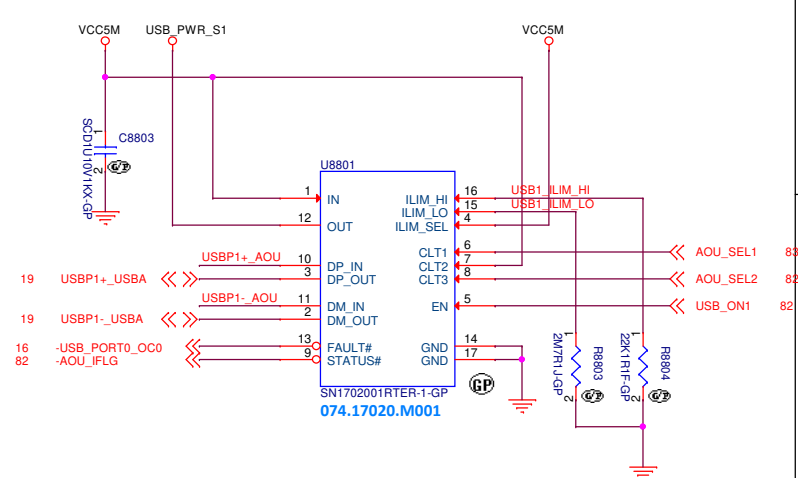


TABLE of USB Charge	
TI	SN1702001RTER (PG1.1)
Pericom	PI5USB2546HZHEX





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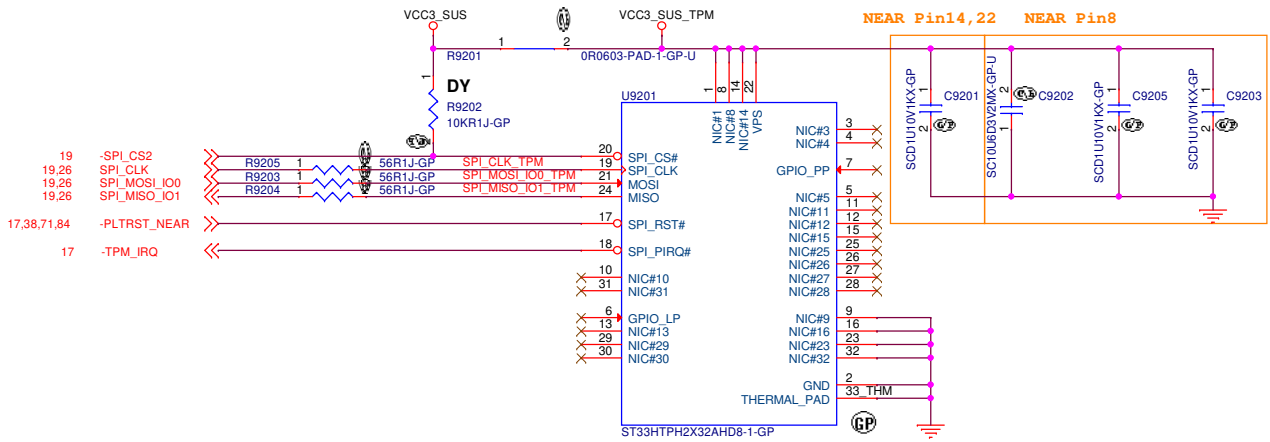
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DISCRETE TPM 2.0



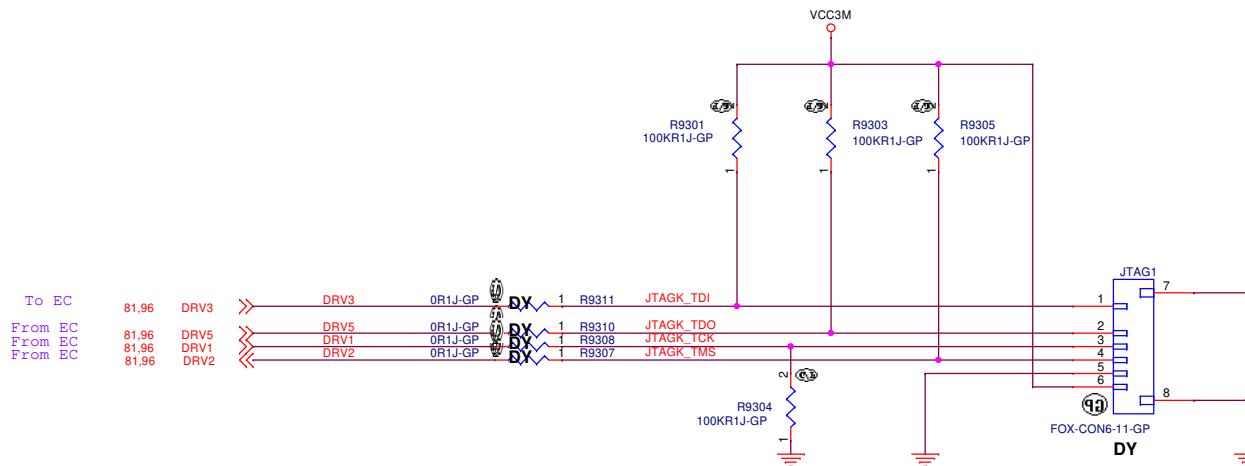
U9201	Vendor P/N	Lenovo P/N	Wistron P/N
Nuvoton	NPCT750LADYX	SL80W59122	071.00750.0H03
ST Micro	ST33HTPH2X32AHD8	SL81A16618	071.33232.M003

TABLE of TPM (U9201)	
Vendor	P/N
NUVOTON	NPCT750LADYX
ST	ST33HTPH2X32AHD8

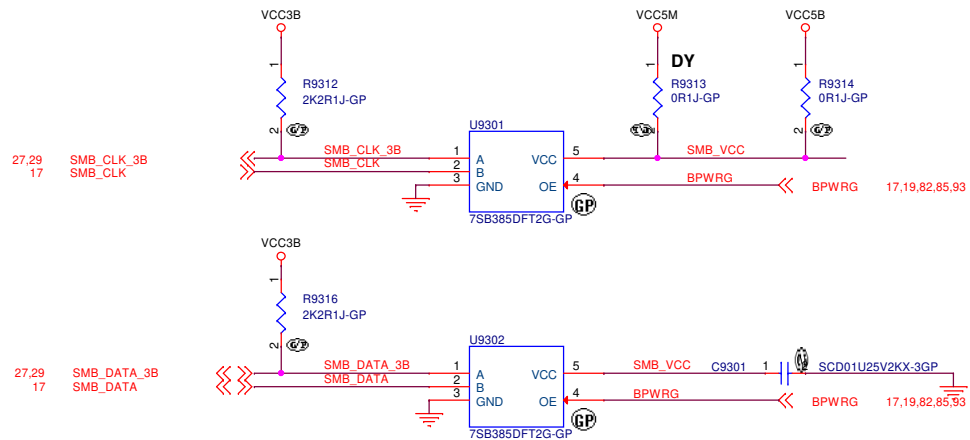
TABLE		
Pin No	NUVOTON NPCT750LADYX SL80W59122	ST Micro ST33HTPH2X32AHD8 SL81A16618
1	VDD	NC
2	NC	GND
3	NC	NC
4	PP	NC
5	NC	NC
6	GPIO3	GPI
7	NC	PP
8	VDD	NiC
9	NC	NC
10	NC	NC
11	NC	NC
12	NC	NC
13	GPIO4	NC
14	NC	NC
15	NC	NC
16	GND	NC
17	RST#	SPI_RST#
18	PIRQ#	SPI_PIRQ#
19	SCLK	SPI_CLK
20	CS#	SPI_CS#
21	MOSI	MOSI
22	VDD	VPS
23	GND	NC
24	MISO	MISO
25	NC	NC
26	NC	NC
27	NC	NC
28	NC	NC
29	SDA/GPIO0	NC
30	SCL/GPIO1	NC
31	NC	NC
32	NC	NC



# LPC/eSPI DEBUG PORT



# SMBUS SWITCH



Close to U43.1 and U43.2

SMB\_CLK\_3B R9315 **DX** 1 0R1J-GP SMB\_CLK

Close to U44.1 and U44.2

SMB\_DATA\_3B R9317 **DX** 1 0R1J-GP SMB\_DATA

BOM1

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Title **SMBUS SWITCH/eSPI DEBUG**

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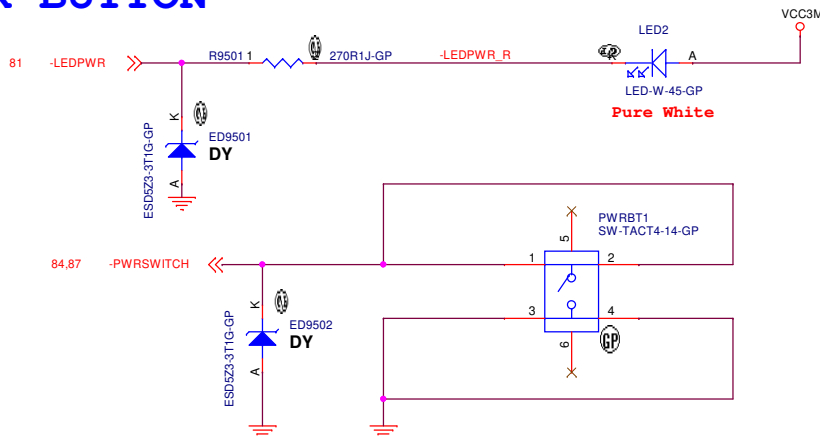
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# PWR BUTTON

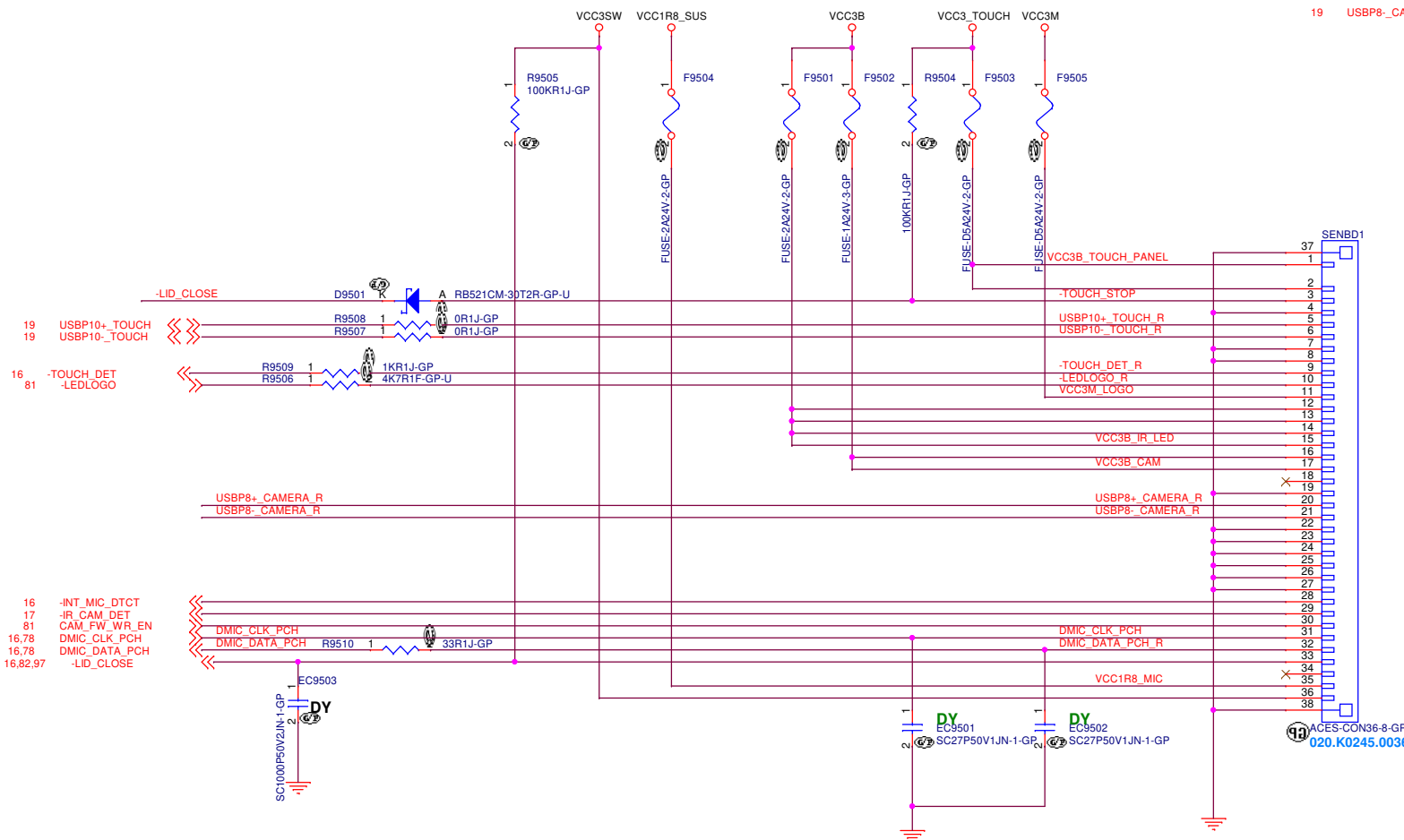


## Near Power SW: SW1

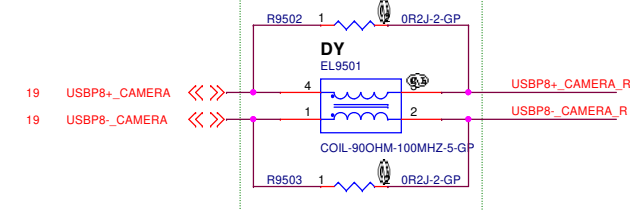
TP9501 TPAD60 1 -PWRSWITCH  
TP9502 TPAD60 1 -PWRSWITCH

TP9503 1 -PWRSWITCH  
TOP side  
Bottom side

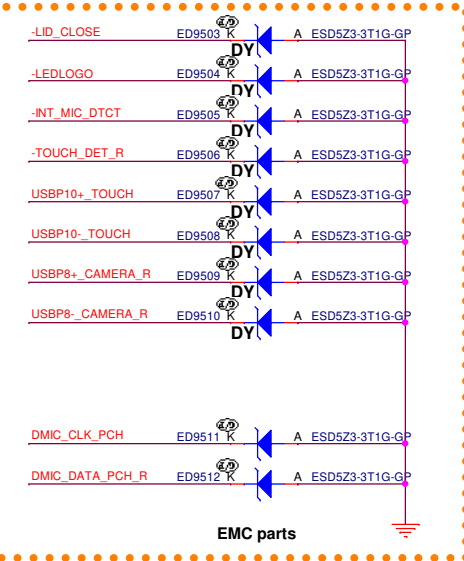
# CAMERA/TOUCH



## Near TOUCH1 CONN Dual Layout



## NEAR TOUCH1 CONN



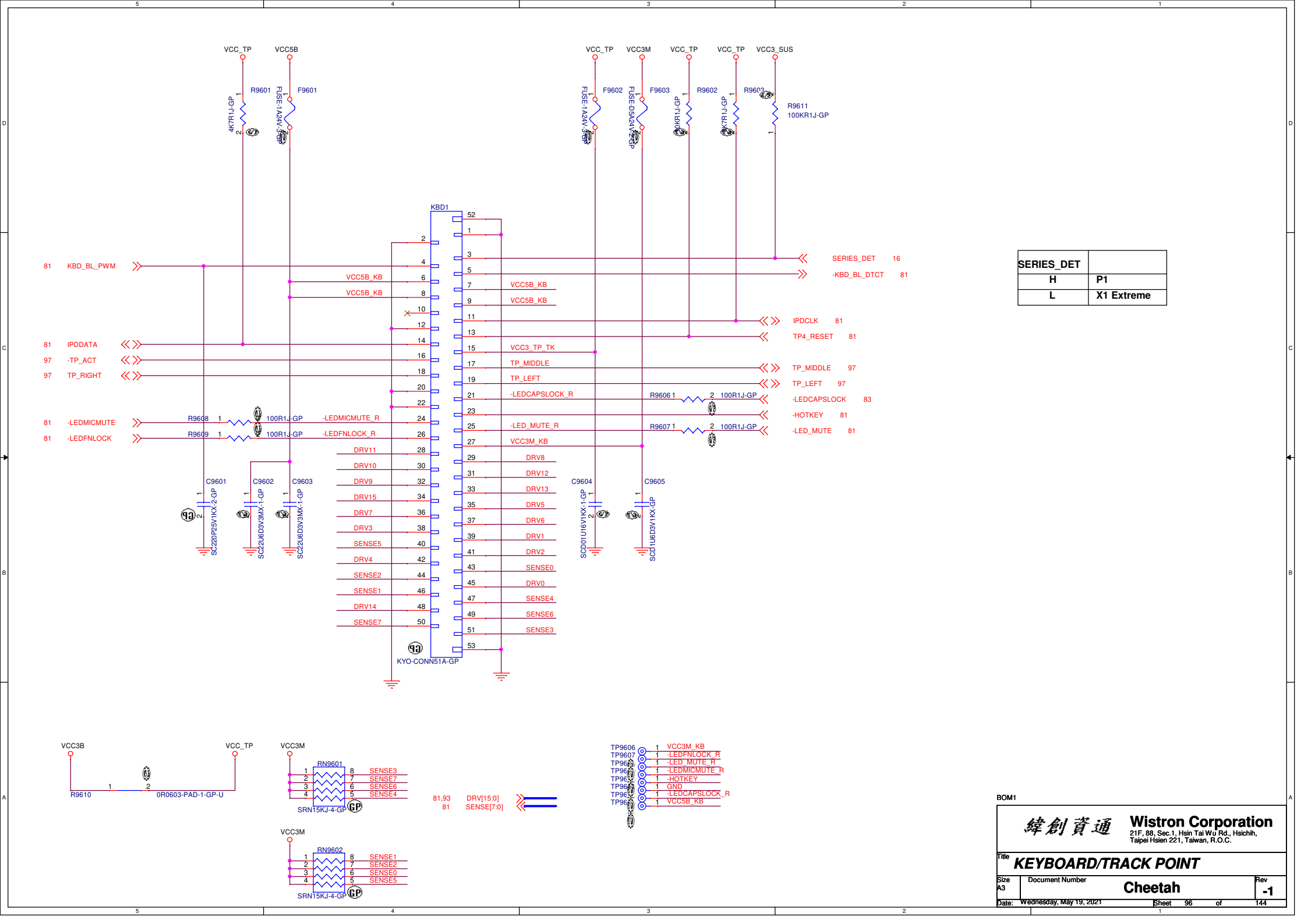
EMC parts

BOM1

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Taipei Hsien 221, Taiwan, R.O.C.

CAMERA/TOUCH/PWR BUTTON			
Title	Document Number	Cheetah	Rev
A3			-1
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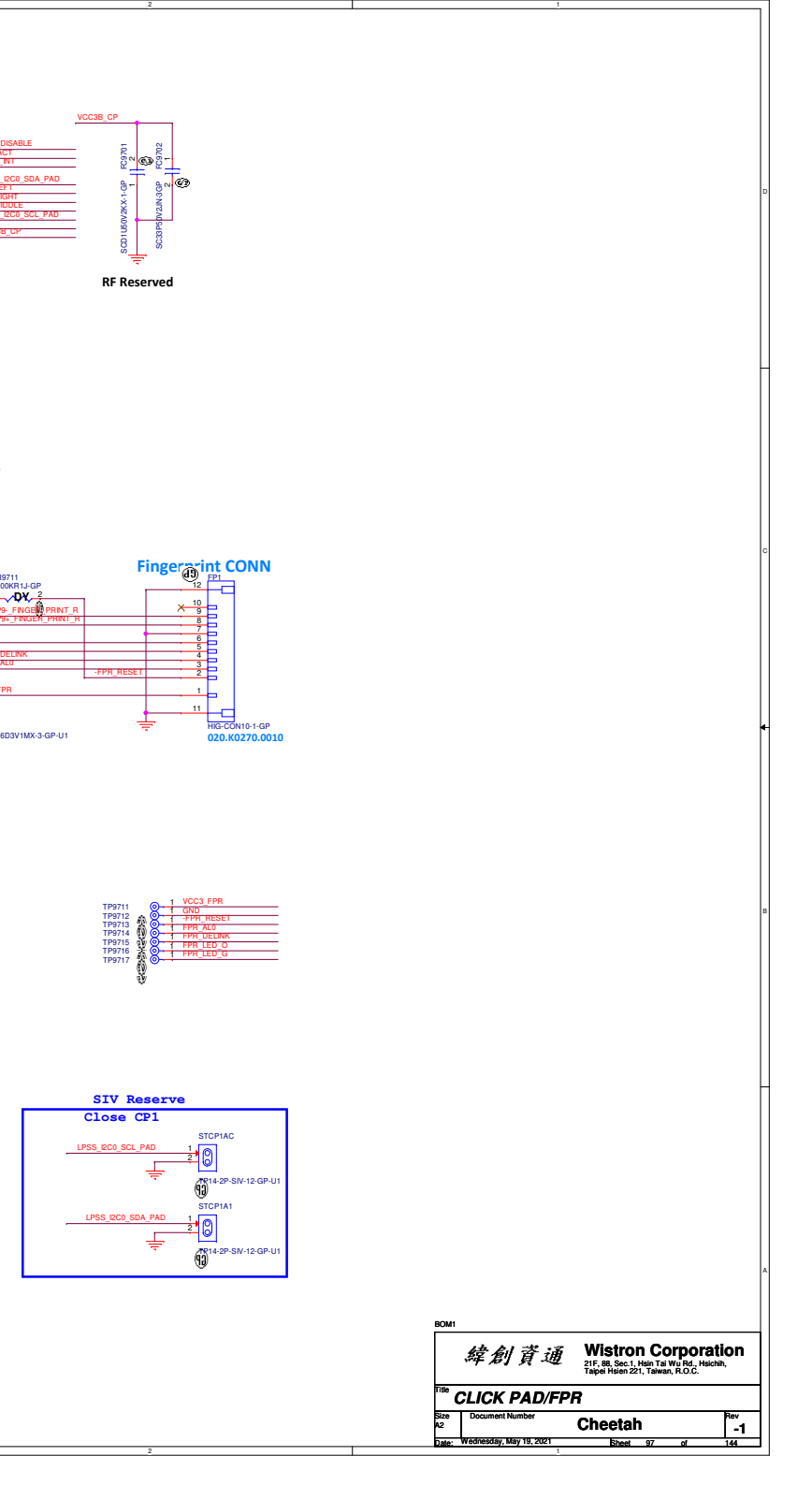
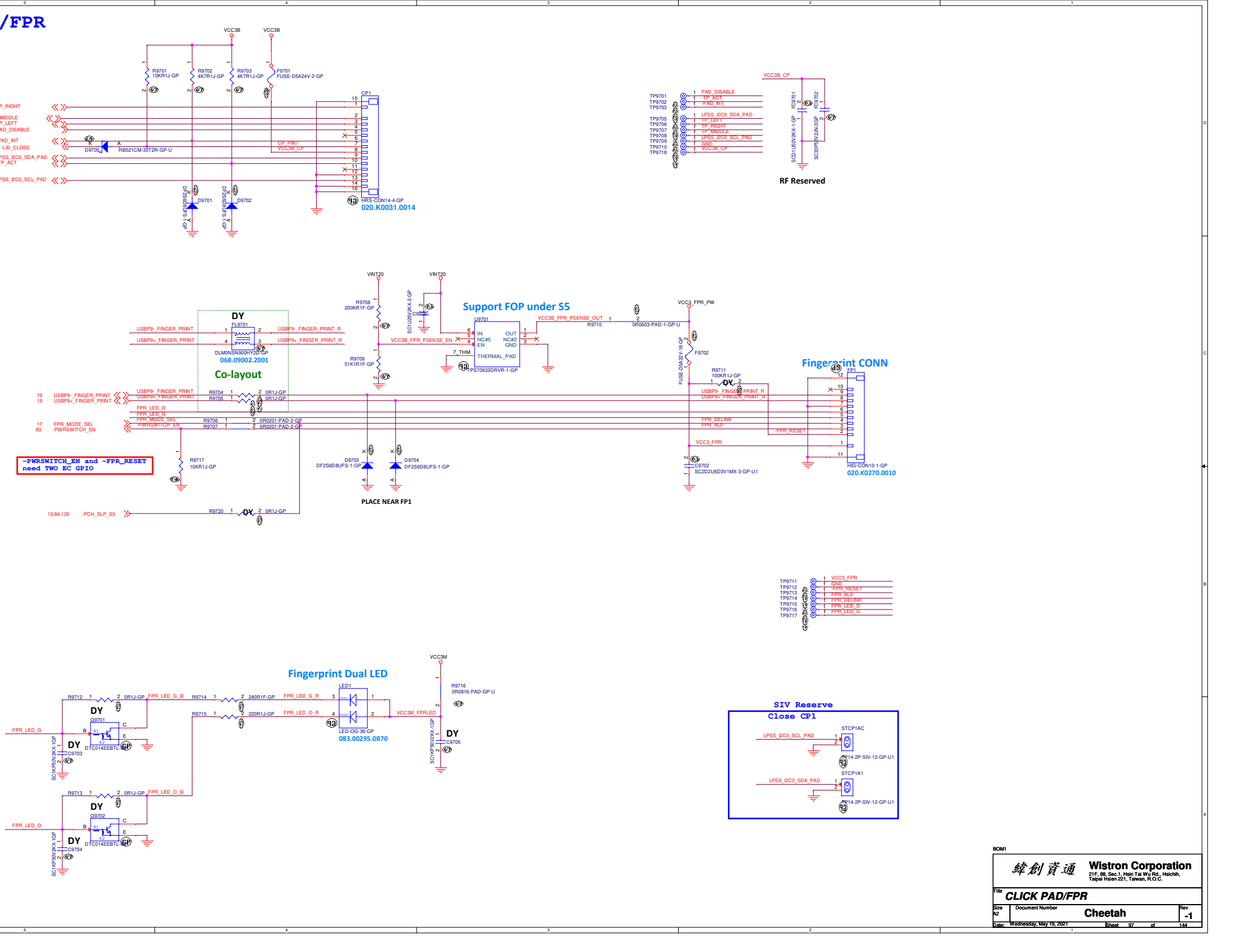
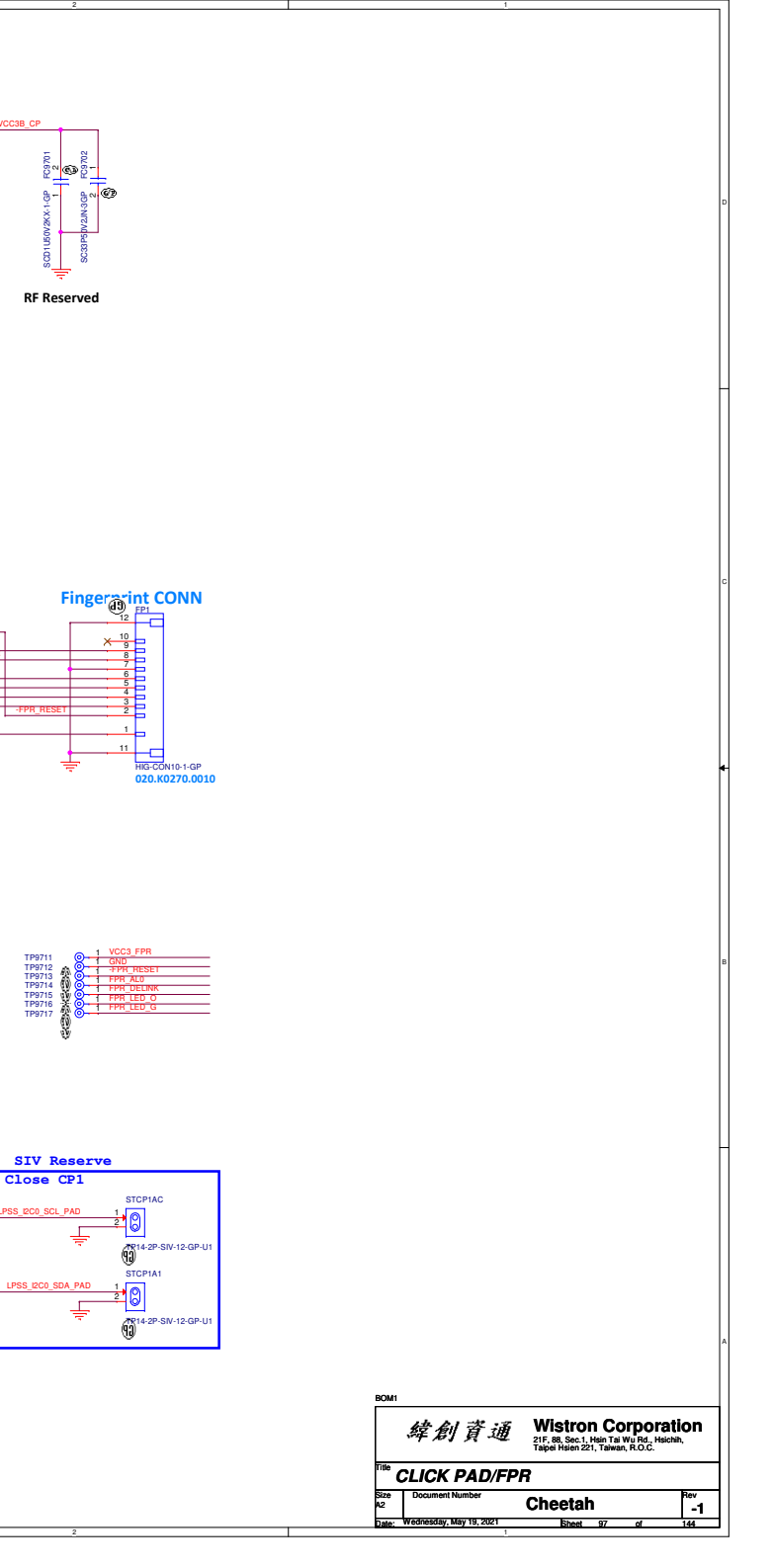
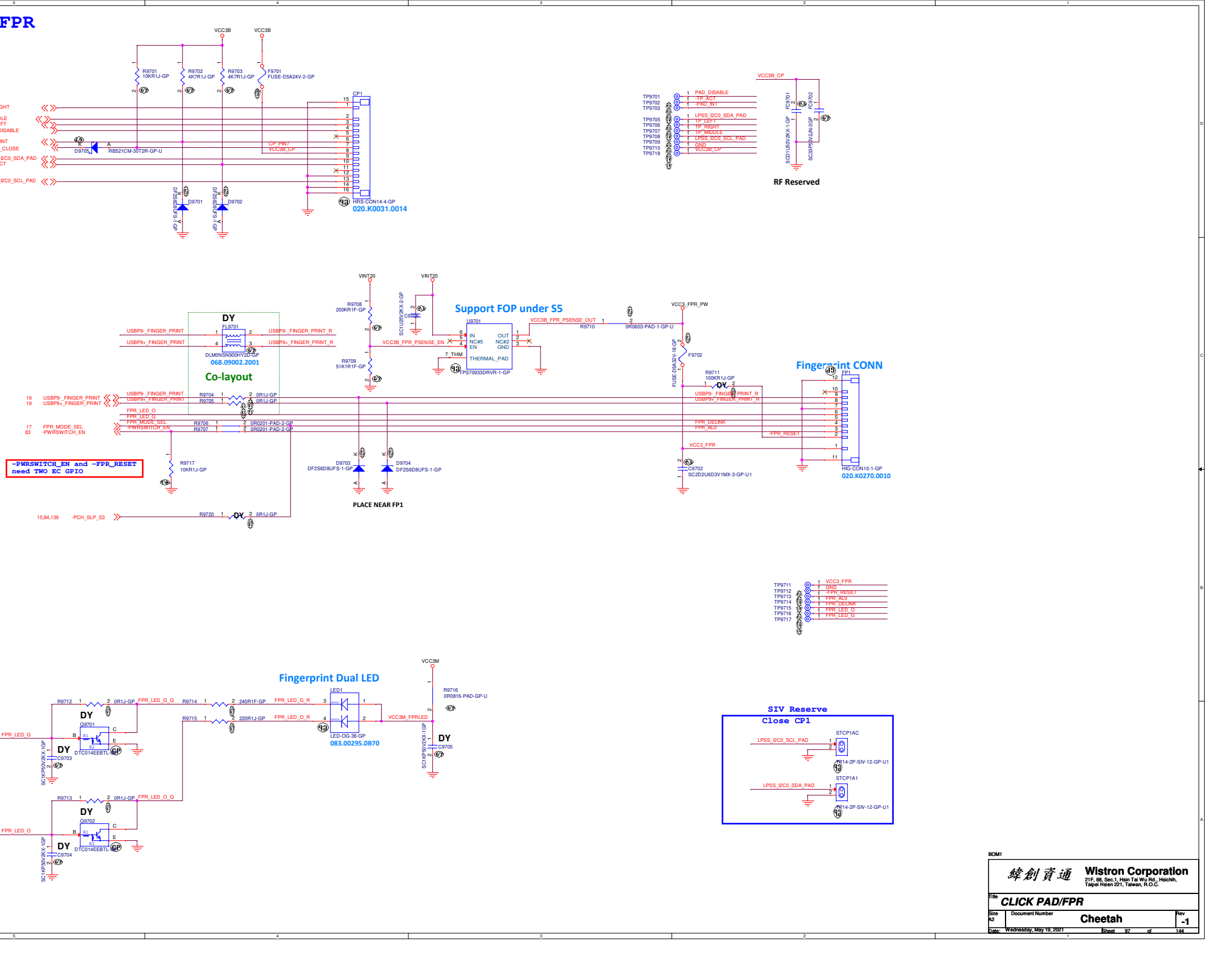
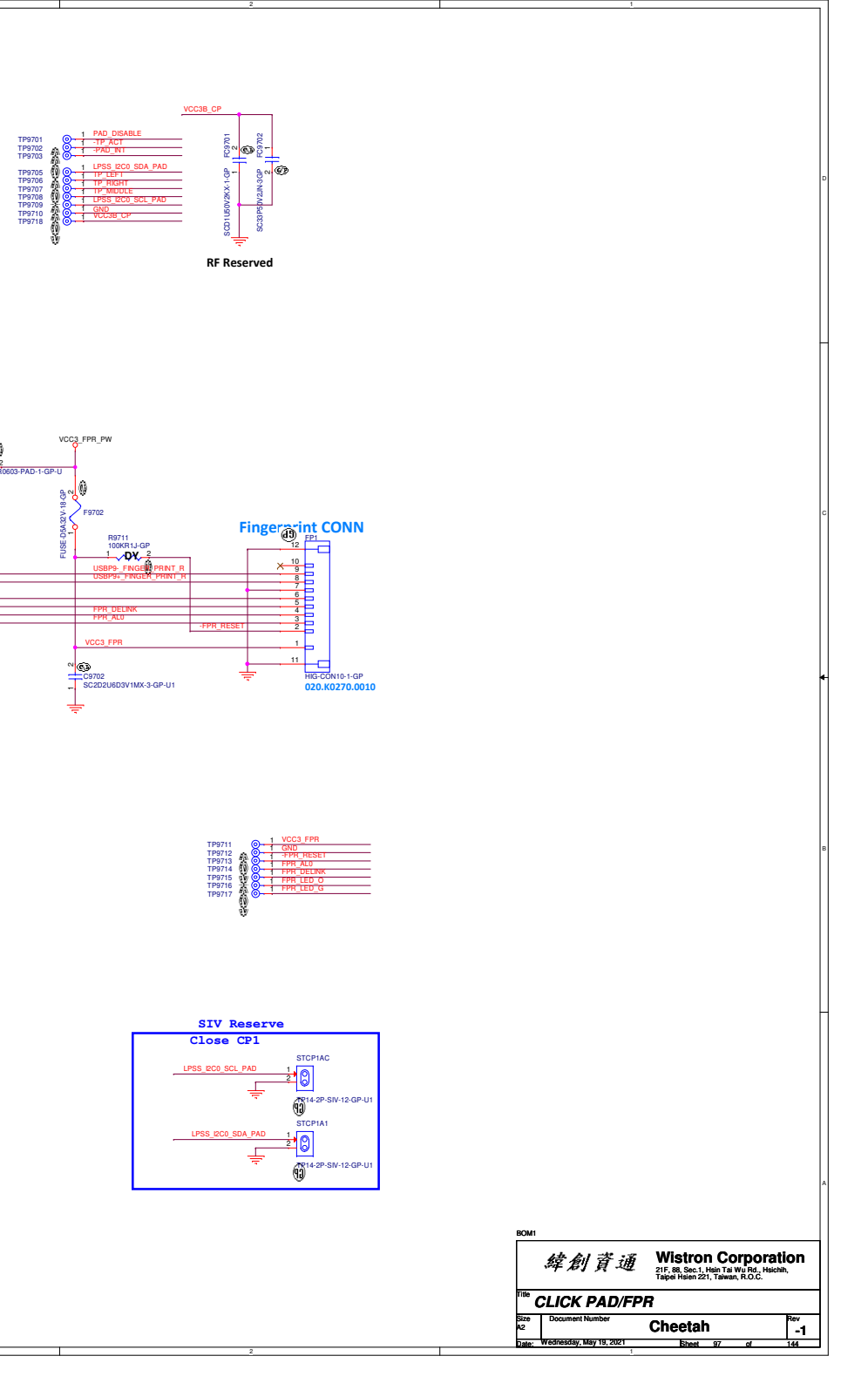
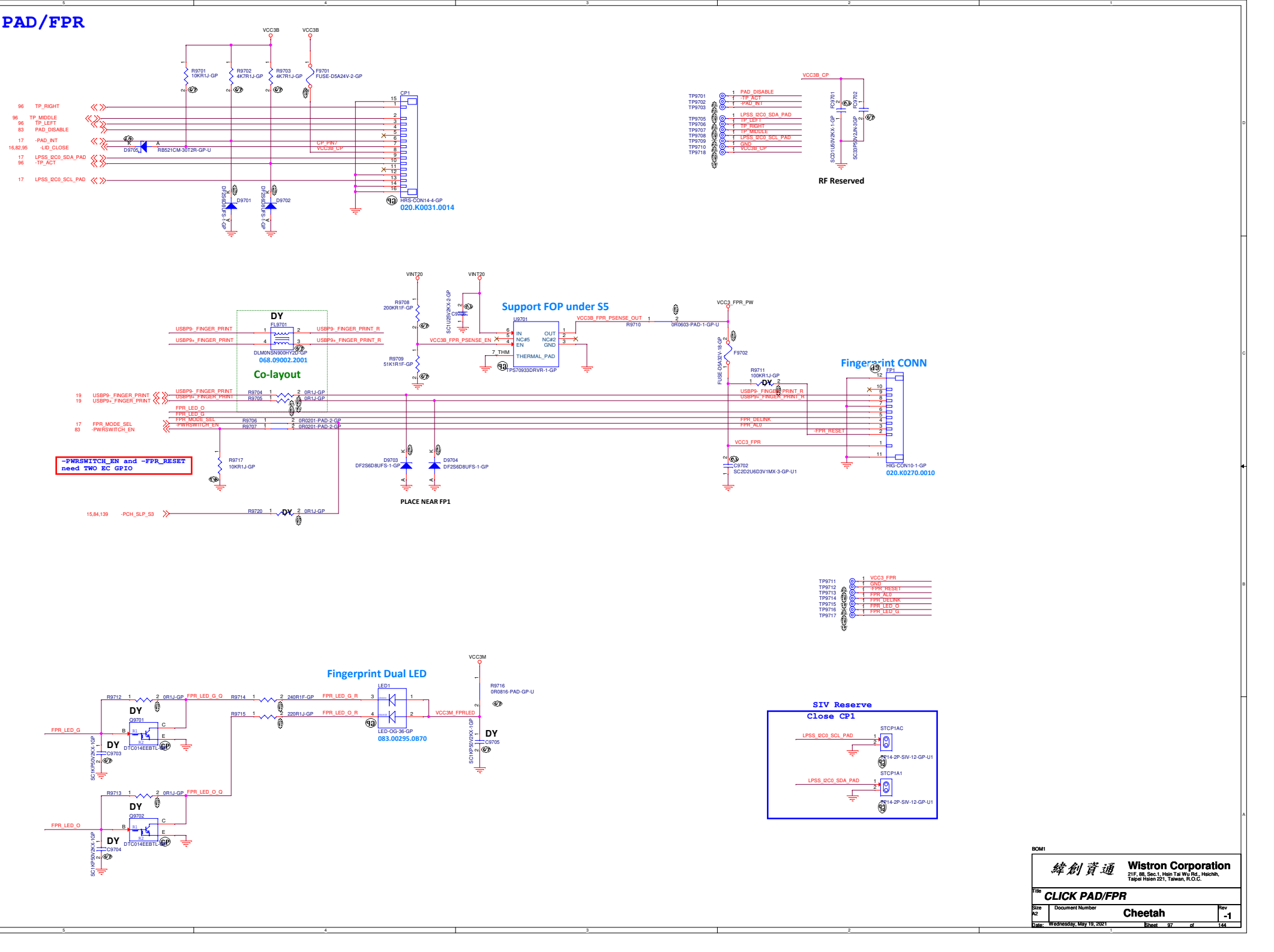




SERIES_DET	
H	P1
L	X1 Extreme

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Title KEYBOARD/TRACK POINT			
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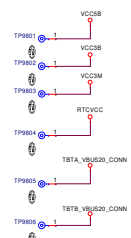
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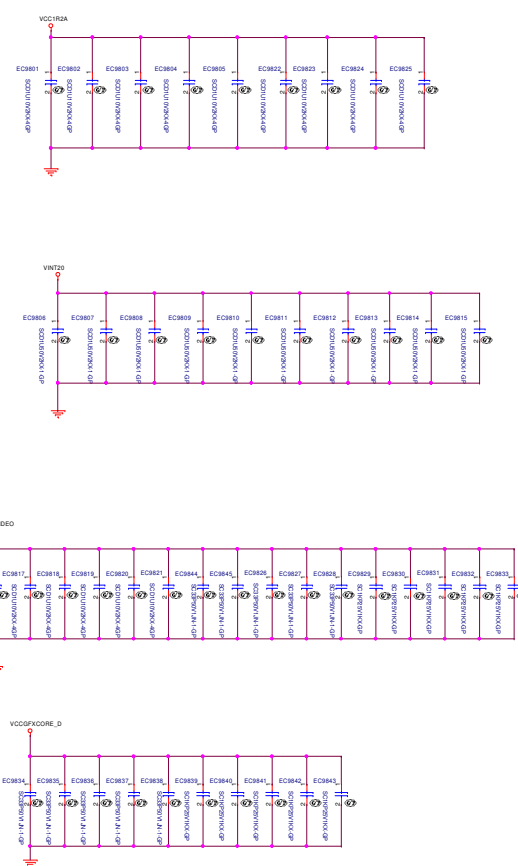
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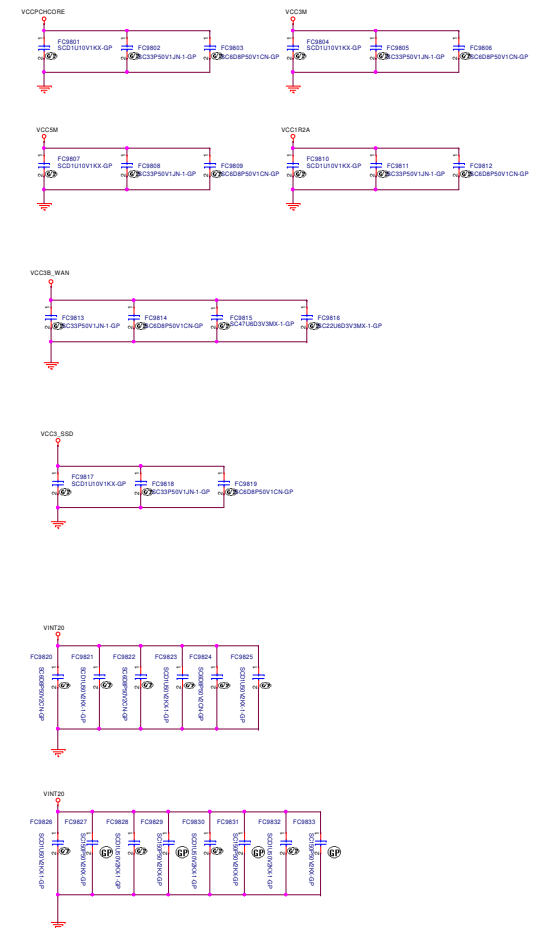
## TEST point



**EMC**

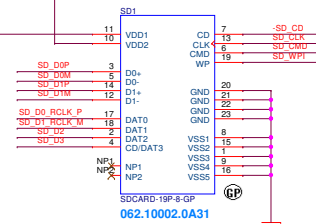
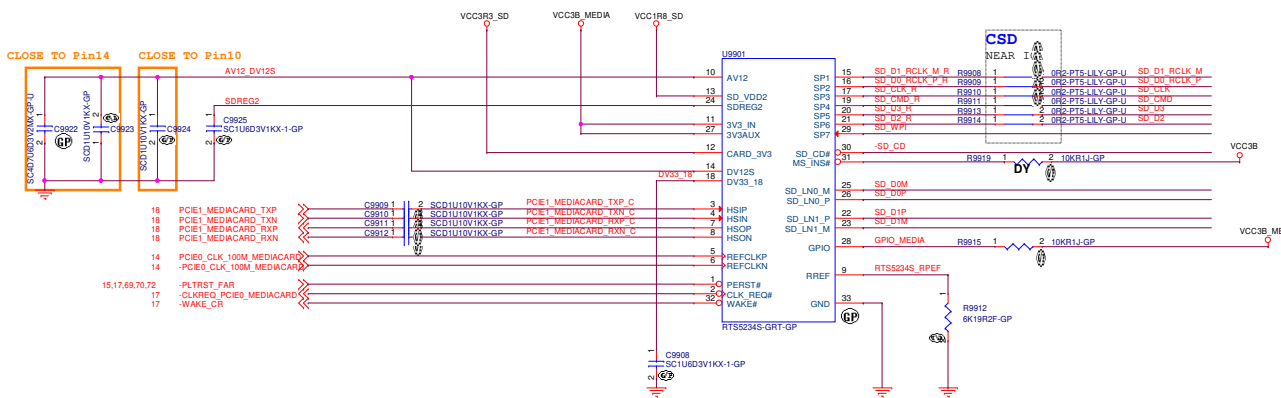


## RF





## SD Card CONN



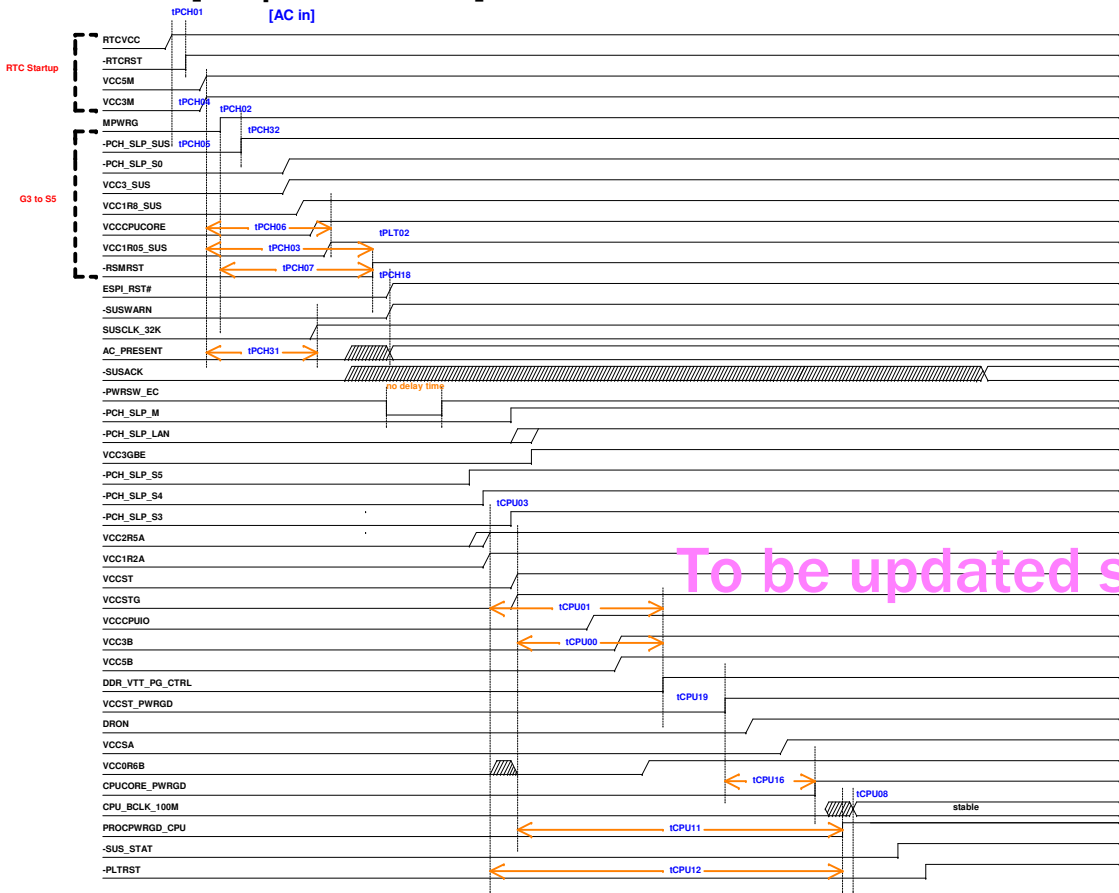
Bottom View

10 1314 17  
1112 1516

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<b>File</b> <b>CARD READER/IO BOARD CONN</b>			
<b>Size</b> Document Number		<b>Cheetah</b>	
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		<b>Rev</b> -1	



CML-H Power On Sequence  
G3 to S0/M0 [Deep Sx Platform]



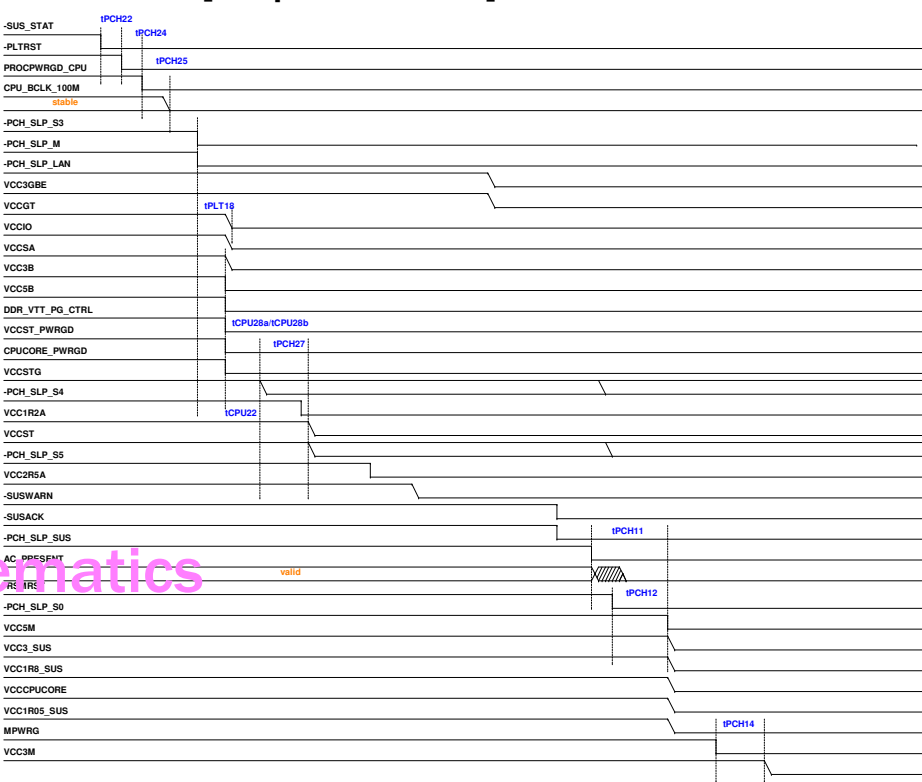
Item	Measure Point	Spec. time	P15/P17 time	Result
IPCH01	RTCVCC To -RTCRST	>9ms	128.5ms	PASS
IPCH04	RTCVCC To VCC3M	>9ms		
IPCH05	-RTCRST To MPWRG	>1us		
IPCH02	VCC3M To -PCH_SLP_SUS	>10ms		
IPCH32	MPWRG To VCC3M	>95ms		
IPCH06	VCC3M To VCC1R8_SUS	>200us		
	VCC3_SUS To VCCCPUCORE			
	VCC1R8_SUS To VCCCPUCORE			
	VCCCPUCORE To VCC1R05_SUS			
	VCC1R05_SUS To -RSMRST		18ms	
IPCH18	-RSMRST To ESPI_RST#	>90us		
IPCH107	MPWRG To -RSMRST	>0ms		
IPCH31	VCC3M To SUSCLK_32K	<105ms		
IPCH03	VCC1R05_SUS To -RSMRST	>10ms		
IPLT02	-RSMRST To ACPRESENT	<0ms		
IPCH15	-PCH_SLP_LAN To VCC3GBE	<20ms		
	-PCH_SLP_S5 To -PCH_SLP_S4			
	-PCH_SLP_S4 To -PCH_SLP_S3			
ICPU03	VCC1R2A To VCCST	<25ms		

Item	Measure Point	Spec. time	P15/P17 time	Result
	VCCST To VCCCPUIO	5.73ms		
	VCCCPUIO To VCC3B	2.43ms		
	VCC3B To VCC5B	2.435ms		
ICPU01	VCC1R2A To VCCST_PWRGD	>1ms	8.66ms	
ICPU00	VCCSTG To VCCST_PWRGD	>1ms	4.89ms	
ICPU11	VCCST To PROCPWRGD_CPU	>1ms	33.6ms	
ICPU19	VCCST_PWRGD To DDR_VTT_CTRL	0~100ms	0s	
ICPU12	VCC1R2A To PROCPWRGD_CPU	<1ms	93ms	
ICPU16	VCCST_PWRGD To CPUCORE_PWRGD	>0ms	21.2ms	
ICPU08	CPU_BCLK_100M To PROCPWRGD_CPU	>1ms	1.015ms	

CPU\_C10\_GATE# sequence (reserved)

tCPU26	All	CPU	PLT	10	65	us	11	CPU_C10_GATE# de-assertion to VCCSTG stable Note: CPU_C10_GATE# de-assertion to VCCST also needs to meet max 65us on cold boot
tCPU27	All	CPU	PLT	10	240	us	11	CPU_C10_GATE# de-assertion to VCCIO stable
tCPU33	All	CPU	PLT		240	us	11	CPU_C10_GATE# de-assertion to VCCPLL_OC stable

CML-H Power Off Sequence  
S0/M0 to G3 [Deep Sx Platform]



Item	Measure Point	Spec. time	P15/P17 time	Result
IPCH22	ESPI_RST# To -PLTRST	>210us		PASS
IPCH24	-PLTRST To PROCPWRGD_CPU	>30us		
IPCH25	PROCPWRGD_CPU To CPU_BCLK_100M	>10us		
IPLT18	-PCH_SLP_S3 To VCCCPUIO	<200us		
ICPU28a	-PCH_SLP_S3 To VCCST_PWRGD	<200us		
ICPU28b	VCCST_PWRGD To VCCST	>0us		
IPCH27	-PCH_SLP_S4 To -PCH_SLP_S5	>30us		
ICPU22	VCCST_PWRGD To VCCSTG	>1us		
IPCH11	-PCH_SLP_SUS To VCC1R05_SUS	>100ns		
IPCH12	-RSMRST To VCC3M	>400ns		
IPCH14	MPWRG To VCC3M	>400ns		







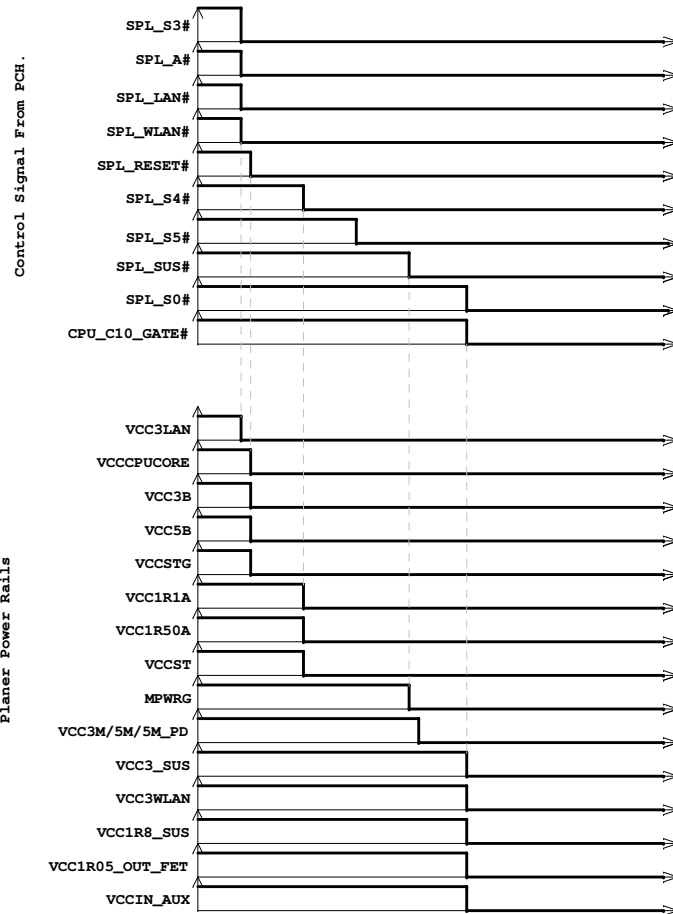
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Timing Diagram for S0/M0 to G3 [Deep Sx]  
Based on planer power rail.



Power Rail Name	Voltage Range	Enable/Control Signal	Sx Power State			
			S0	S3	S4	S5
VINT20	9-20V	NA	ON	ON	ON	ON
RTCVCC	3-3.3V	NA	ON	ON	ON	ON
VCC3SW	3.3V	NA	ON	ON	ON	ON
VCC3M	3.3V	M_ON	ON	ON	ON	ON
VCC3LAN	3.3V	VCC3LAN_DRV	ON	OFF	OFF	OFF
VCC3_SUS	3.3V	SUS_DRV	ON	ON	ON	ON
VCC3WLAN	3.3V	NA	ON	ON	ON	ON
VCC3B	3.3V	VCC3B_DRV	ON	OFF	OFF	OFF
VCC3P	3.3V	VCC3P_DRV	ON	OFF	OFF	OFF
VCC5M	5V	M_ON	ON	ON	ON	ON
VCC5B	5V	VCC5B_DRV	ON	OFF	OFF	OFF
VCC1R8_SUS	1.8V	VCC3_SUS-PWRGD	ON	ON	ON	ON
VCC1R8A	1.8V	-CPU_C10_GATE	ON	ON	ON	ON
VCCPCHCORE	2 bit VID	V1R8_SUS_PWRGD	ON	ON	ON	ON
VCCST	1.05V	VCCST_OVERRIDE OR -PCH_SLP_S3	ON	OFF	OFF	OFF
VCCSTG	1.05V	VCCST_OVERRIDE OR -CPU_C10_GATE	ON	OFF	OFF	OFF
VCCCPUCORE	SVID	CPUCORE_ON	ON	OFF	OFF	OFF
VCC1R1A	1.1V	-PCH_SLP_S4	ON	ON	OFF	OFF
VCC5R0A	5V	-PCH_SLP_S4*	ON	ON	OFF	OFF
VCC5M_PD	5V	M_ON	ON	ON	ON	ON
VCC1R1_PCON	1.1V	TBD				

Not fixed yet.  
Please refer to latest TGL-H PDG.



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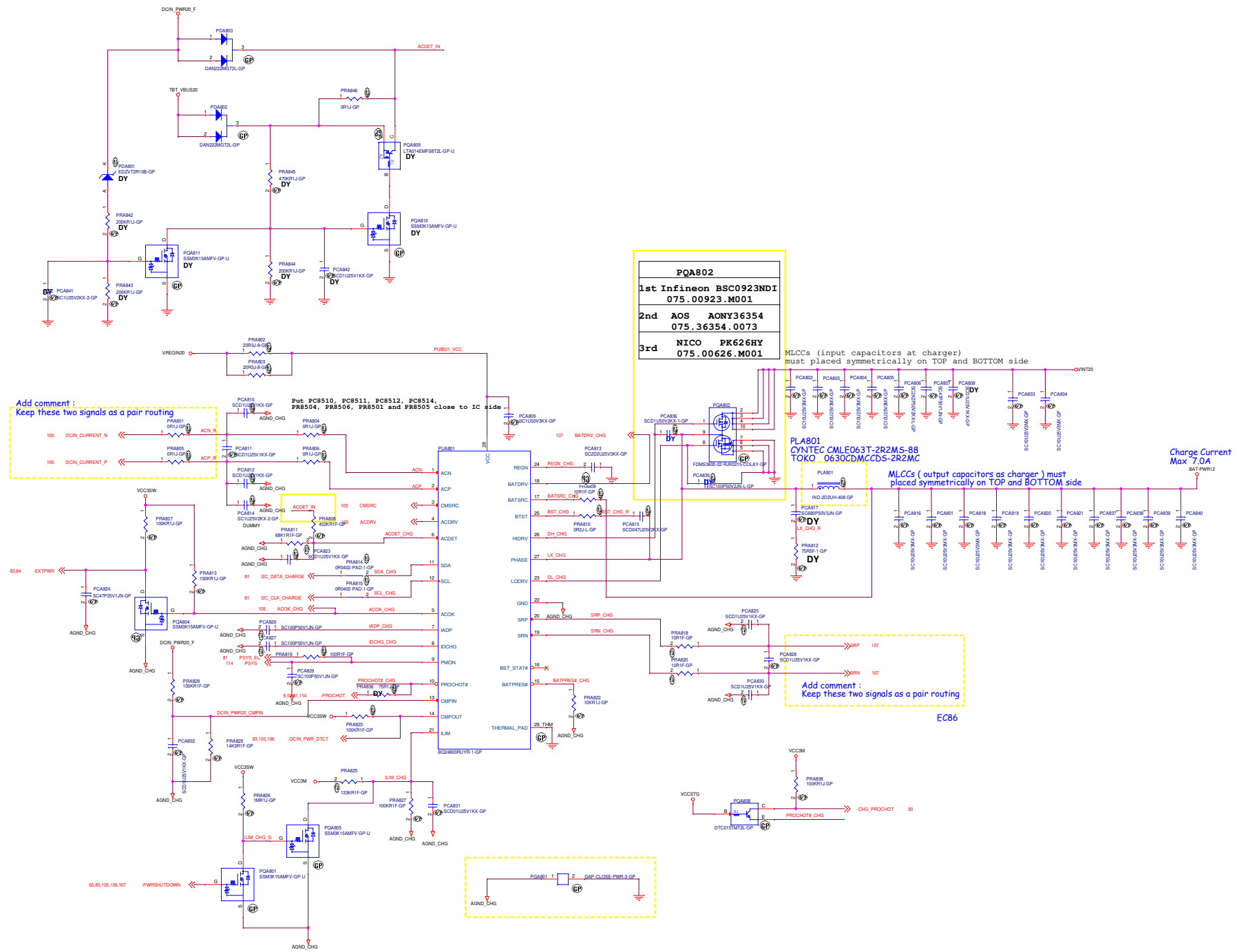












PQAB2	
1st	Infineon BSC0923NDI 075.00923.M001
2nd	AOS AONY36354 075.36354.0073
3rd	NICO PK626HY 075.00626.M001

MLCCs (input capacitors at charger)  
must be placed symmetrically on TOP and BOTTOM side

PLA801  
CYNTEC CMLE063T-2R2MS-88  
TOKO\_0630CDMCCDS-2R2MC

Charge Current  
Max 7.0A

Add comment:  
Keep these two signals as a pair routing

EC86



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keep more than 2.0mm height for  
if acoustic noise suppression MLCC use

Add comment :  
MLCCs (Input capacitors at charger)  
must placed symmetrically on TOP and BOTTOM side

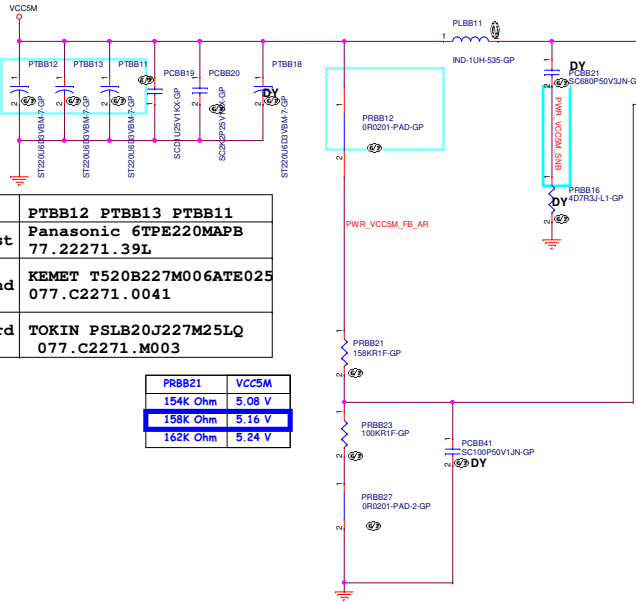
PQBB11		
1st	Infinion	BSC0923NDI 075.00923.M001
2nd	AOS	AONY36354 075.36354.0073
3rd	NICO	PK626HY 075.00626.M001

VCC5M  
Max 15.3A  
Cont 9.0A

Dual-N standard symbol to colay

PQBB11

Table PLBB11	CYNTEC	CMLS063T-1R0M5-88	068.1R010.2591
	SUMIDA	0630CDMCD05-1R0MC	068.1R010.1H11



	PTBB12	PTBB13	PTBB11
1st	Panasonic	6TPE220MAPB	77.22271.39L
2nd	KEMET	T520B227M006ATE025	077.C2271.0041
3rd	TOKIN	PSLB20J227M25LQ	077.C2271.M003

PRBB21	VCC5M
154K Ohm	5.08 V
158K Ohm	5.16 V
162K Ohm	5.24 V

PQBB12

1st	Infinion	BSC0923NDI 075.00923.M001
2nd	AOS	AONY36354 075.36354.0073
3rd	NICO	PK626HY 075.00626.M001

keep more than 2.0mm height for  
if acoustic noise suppression MLCC use

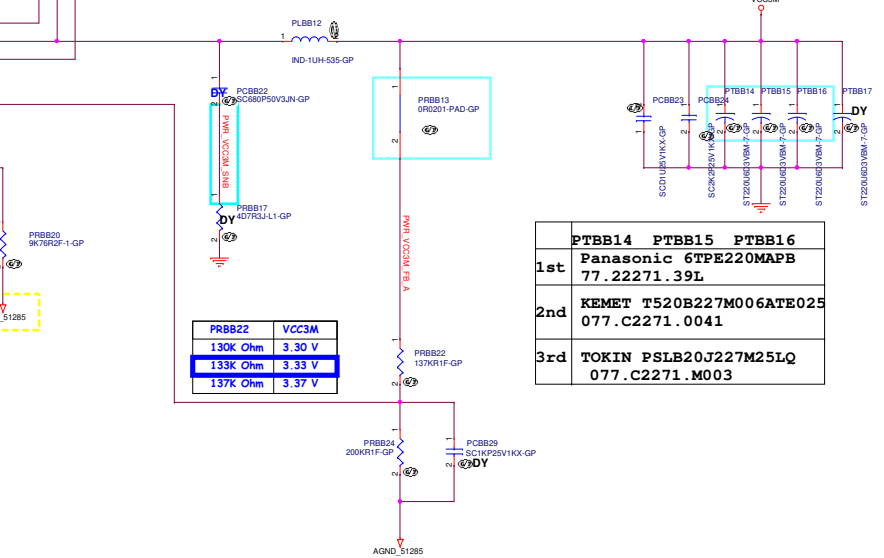
Add comment :  
MLCCs (Input capacitors at charger)  
must placed symmetrically on TOP and BOTTOM side

VCC3M  
Max 15.0A  
Cont 12.3A

Dual-N standard symbol to colay

PQBB12

Table PLBB12	CYNTEC	CMLS063T-1R0M5-88	068.1R010.2591
	SUMIDA	0630CDMCD05-1R0MC	068.1R010.1H11



PRBB22	VCC3M
130K Ohm	3.30 V
133K Ohm	3.33 V
137K Ohm	3.37 V

	PTBB14	PTBB15	PTBB16
1st	Panasonic	6TPE220MAPB	77.22271.39L
2nd	KEMET	T520B227M006ATE025	077.C2271.0041
3rd	TOKIN	PSLB20J227M25LQ	077.C2271.M003

BOB1



	PLB101
1st	CMLE063T-R47MS-88
2nd	0630CDMCCDS-R47MC 068.R4710.1A41

**VCC1R2A**





Vin: 12V~20V

**PLB201**  
**1st TOKO DFE252012F-1R0M=P2**  
**068.1R010.1791**  
**2nd CYNTEC HMLQ25201B-1R0MSR-88**

2.5V/1.4A

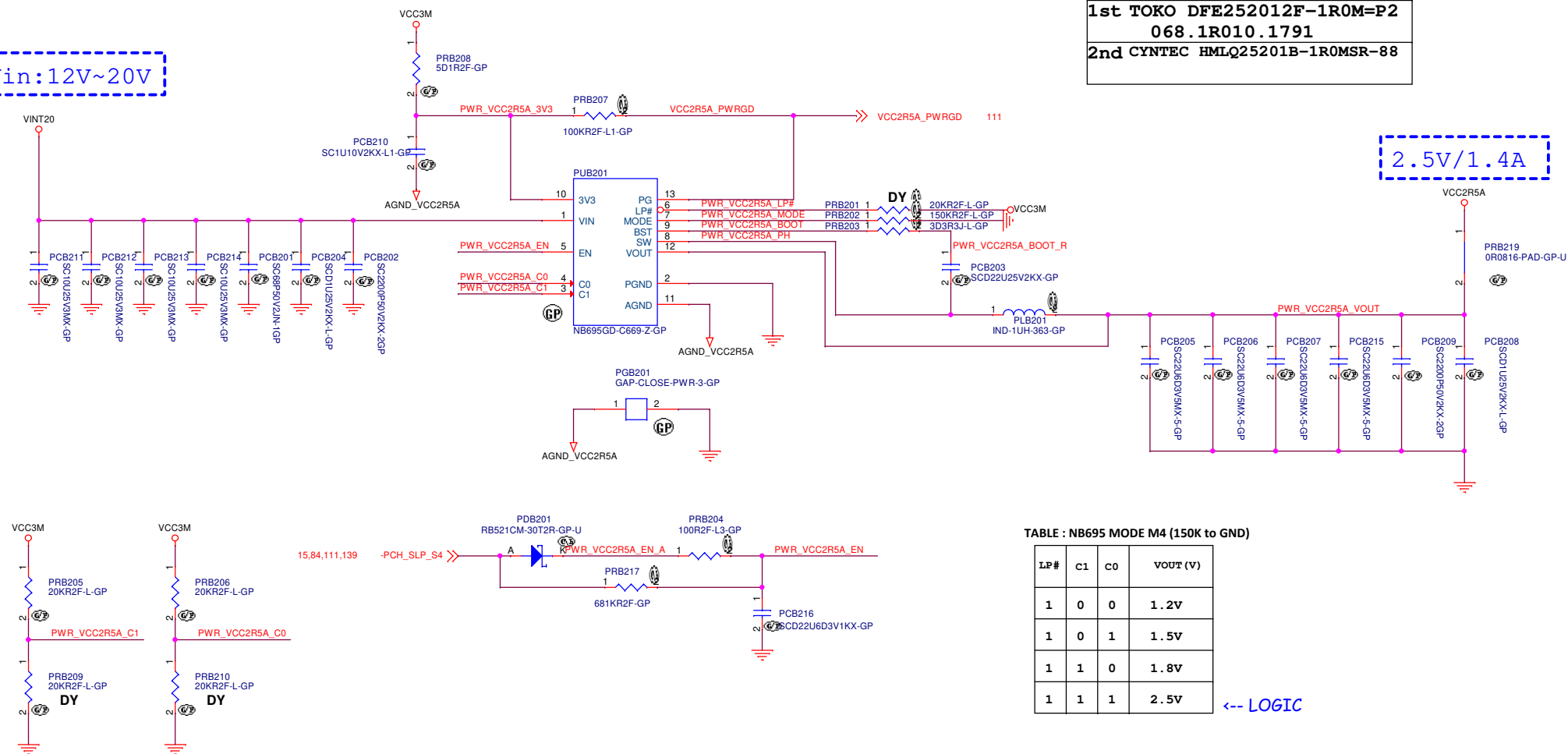


TABLE : NB695 MODE M4 (150K to GND)

LP#	C1	C0	VOUT (V)
1	0	0	1.2V
1	0	1	1.5V
1	1	0	1.8V
1	1	1	2.5V

← LOGIC

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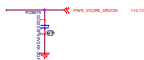
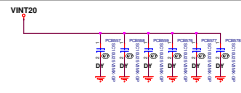
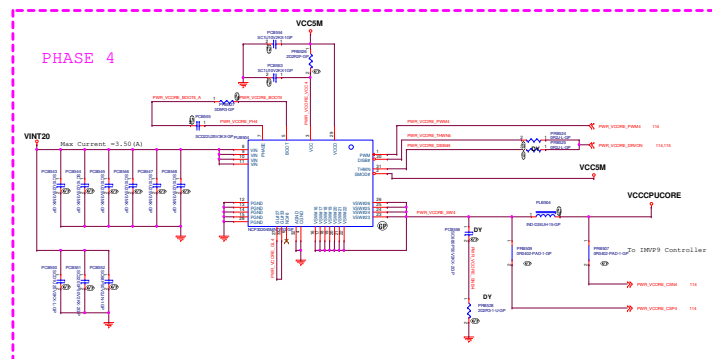
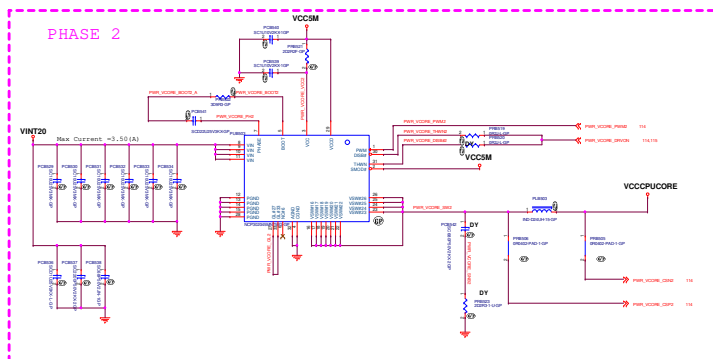
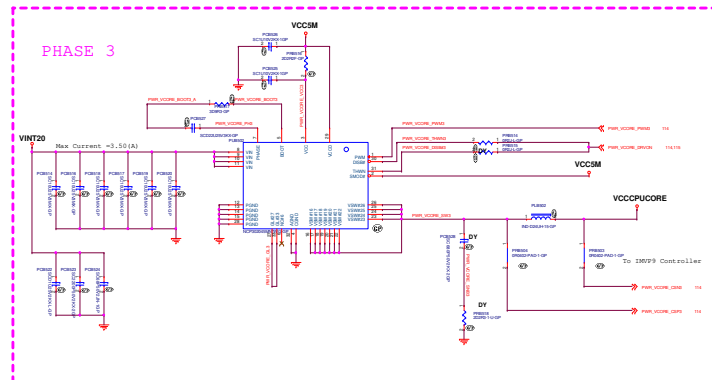
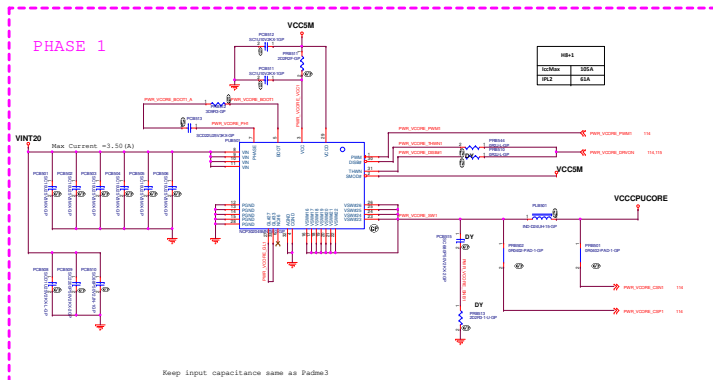


TABLE of PWR01, PWR02, PWR03, PWR04, PWR05			
VENDOR	P/N	MAXIMUM P/N	MAXIMUM P/N
1st	ON SEMI	MT06M015007PWS	68A 42415.1001
2nd	ADG	ADG111402	68A 42415.1001

TABLE of PWR01, PWR02, PWR03, PWR04, PWR05			
VENDOR	P/N	MAXIMUM P/N	MAXIMUM P/N
1st	CYRTEC	CM4045T 42415.1007-68	68A 42415.1001
2nd	Samida	68A42415.1001	68A 42415.1001





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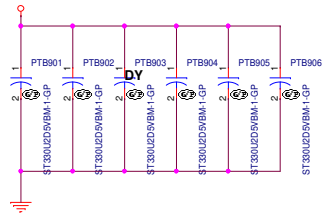
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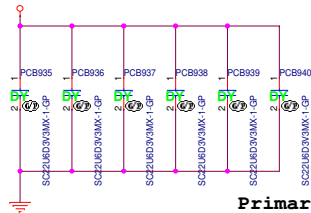


Place close to VR

VCCCPUCORE



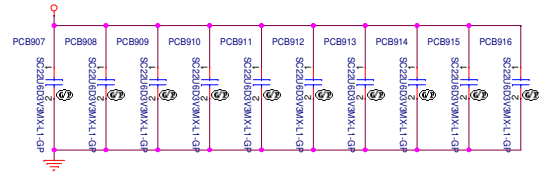
VCCCPUCORE



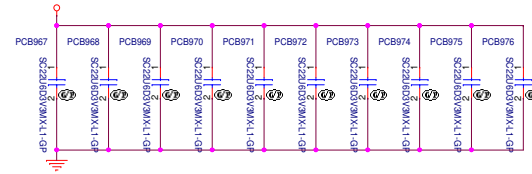
Primary Caps :  
330uF \*6 = 1980uF

Place close to CPU

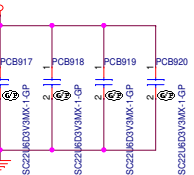
VCCCPUCORE



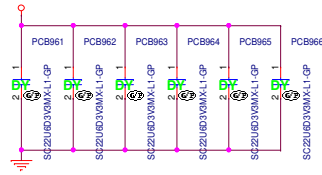
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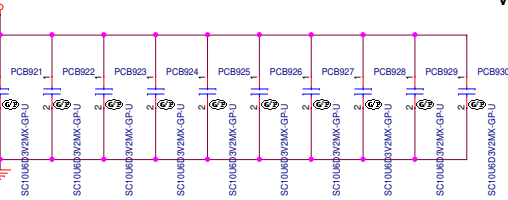
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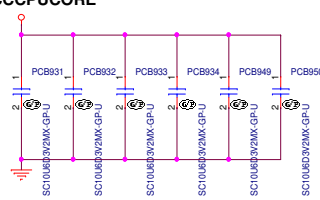
VCCCPUCORE



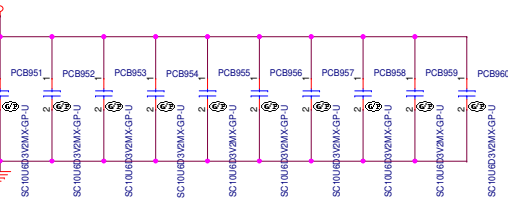
VCCCPUCORE



VCCCPUCORE



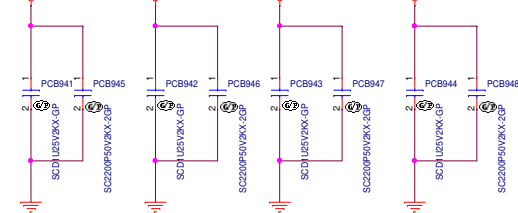
VCCCPUCORE



Secondary Caps : 22uF \*24 + 10uF \*26= 788uF

EMC @ Each Phase

VCCCPUCORE VCCCPUCORE VCCCPUCORE VCCCPUCORE



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File VCCPUCORE DECOUPLING

Size C Document Number

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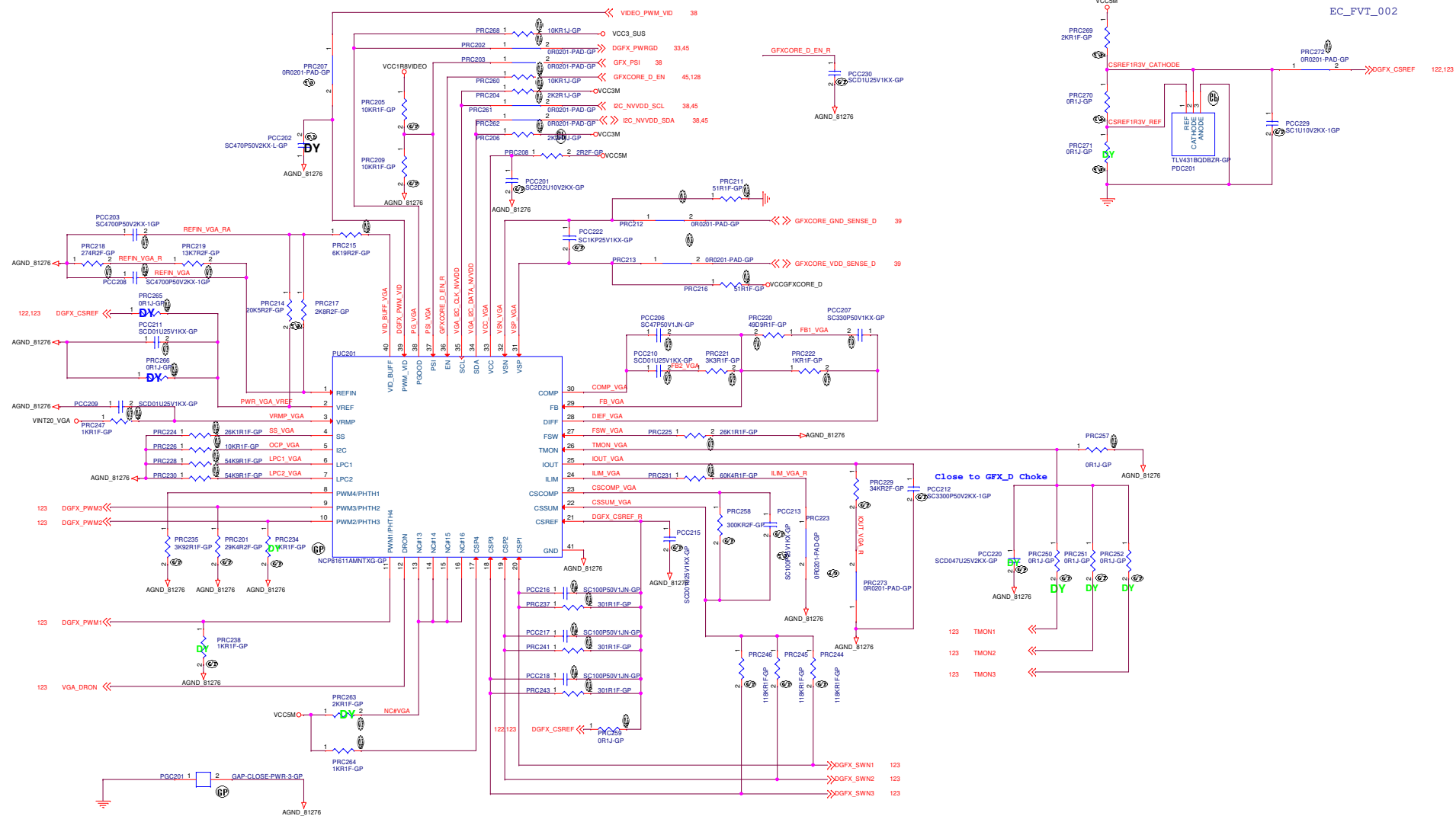






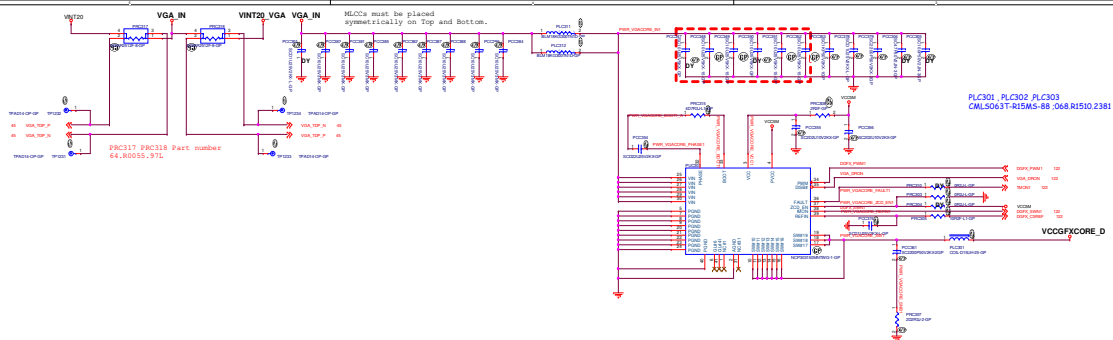






PRC217	PRC218	PRC219	Vboot	
2.8K	274	13.7K	0.75V	GN20x/QN20x
4.12K	2.74K	13.7K	0.8V	QN20-P1





### POWER SOLUTION

GPU	SKU	GN20-E7/E5/E4	GN20-E3	GN20-P1/P0
Frame Buffer & FBVDD VR Solution	# FBVDD VR Phases	2	2	1
	FBVDD VR Efficiency (%)	Minimum: 90, Target: 94		
	Legacy PSl support for Lower Power Mode	Required		
Core Power Solution	# Core VR Phases	4 @ 80W (5 @ 115W)	3 @ 60W (4 @ 80W, 5 @ 115W)	2 @ 35W (3 @ 60W)
	VR Efficiency (%)	Minimum: 87, Target: 91		
	Idle Efficiency (%)	Minimum: 80		
	AutoPSl support for Lower Power Mode	Required		
	Idle Efficiency (%)	Minimum: 85, Target: 90		
1VB/PEX Power rails	Idle Efficiency (%)	Minimum: 85, Target: 90		

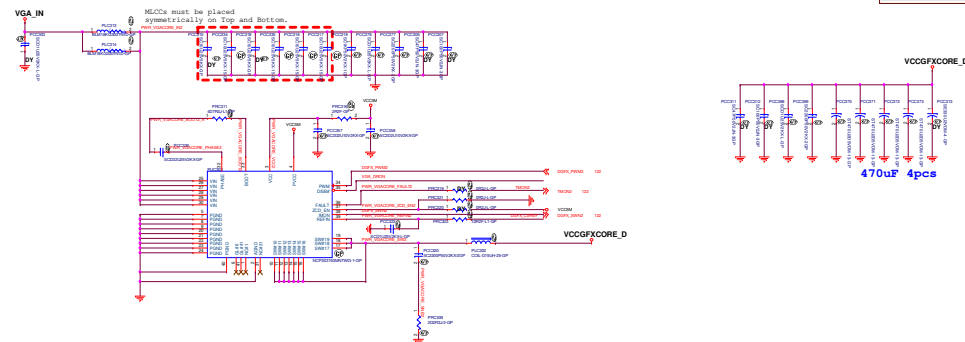
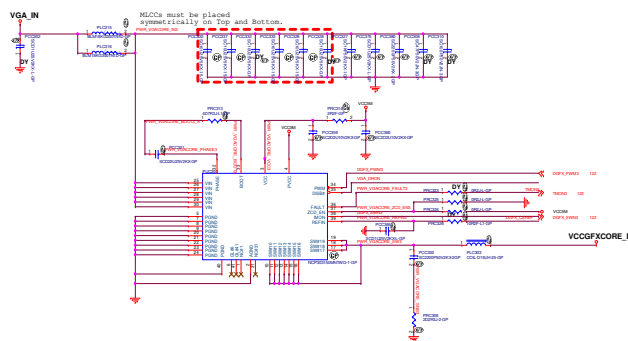


TABLE OF P1C301, P1C302, P1C303		
VENDOR	PIN	MINIMUM PIN
1A	100	100
2A	100	100





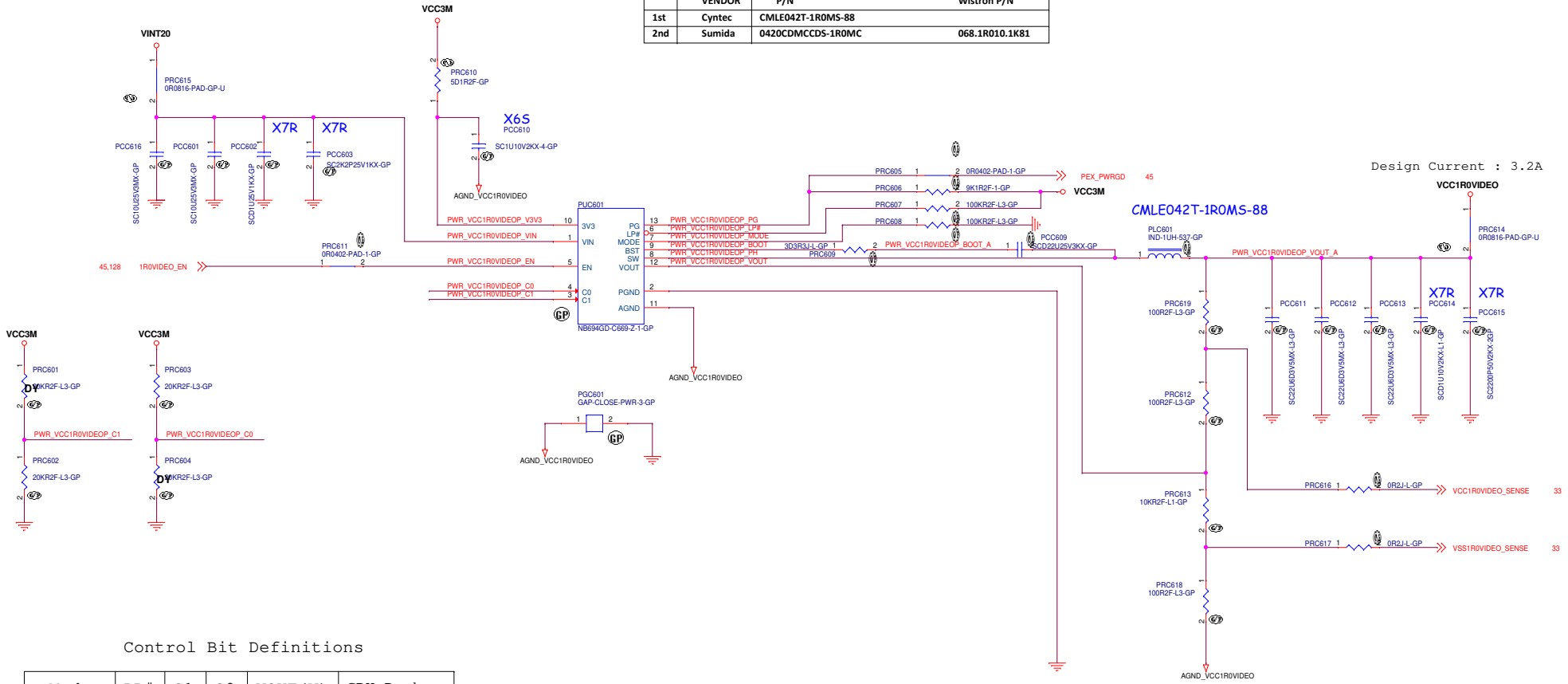
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TABLE of PLC601			
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1st	Cyntec	CMLE042T-1R0MS-88	
2nd	Sumida	0420CDMCCDS-1R0MC	068.1R010.1K81

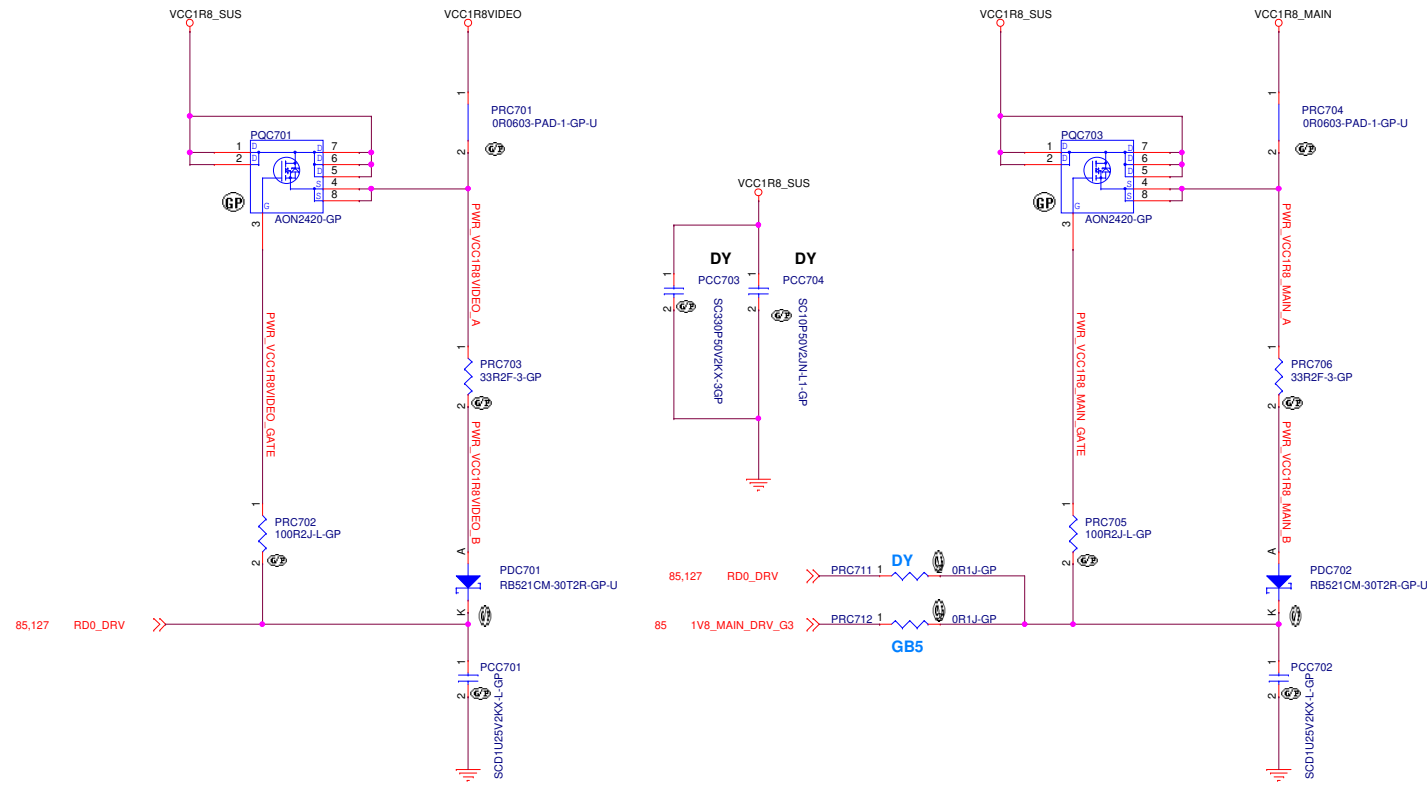


Control Bit Definitions

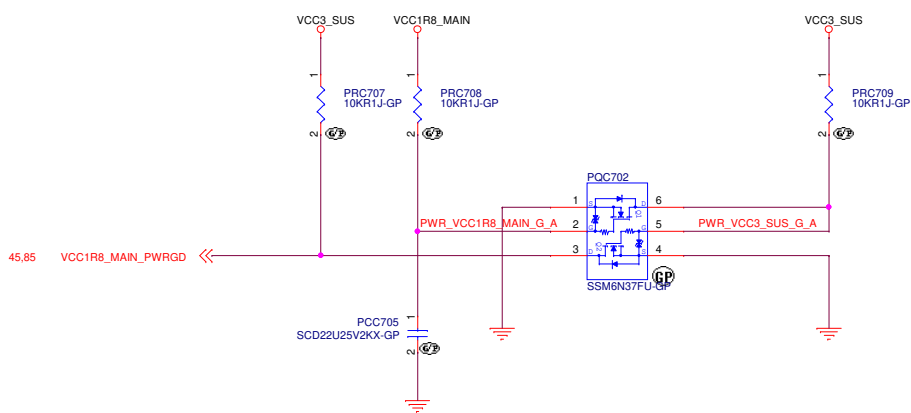
Mode	LP#	C1	C0	VOUT (V)	GPU Package
100Kohm	0	X	X	0V	
	1	0	0	0.8V	
	1	0	1	0.95V	GB5B-128
	1	1	0	1V	GB5-128
	1	1	1	1.05V	

	PRC616	PRC617	PRC612	PRC618	PRC619	PRC613
GB5-128 (QN20P-Q1)	ASM	ASM	100R	100R	100R	10K
GB5B-128 (QN20P-Q3)	No-ASM	No-ASM	0R	0R	0R	200K





	PRC712	PRC711
GB5-128 (QN20P-Q1)	ASM	No-ASM
GB5B-128 (QN20P-Q3)	No-ASM	ASM



	PCC705
GB5-128 (QN20P-Q1)	ASM
GB5B-128 (QN20P-Q3)	No-ASM

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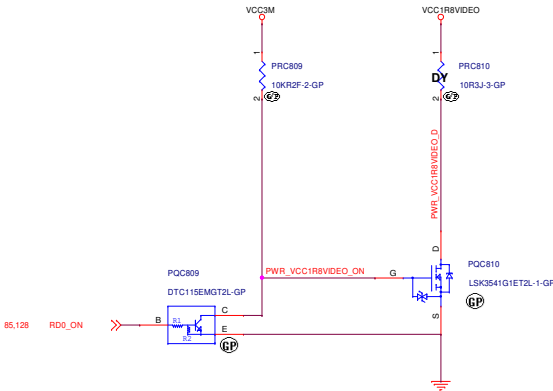
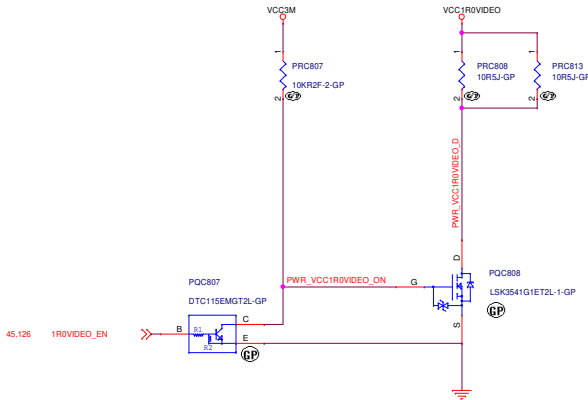
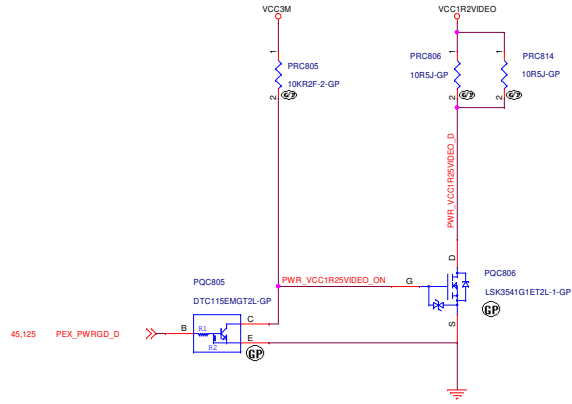
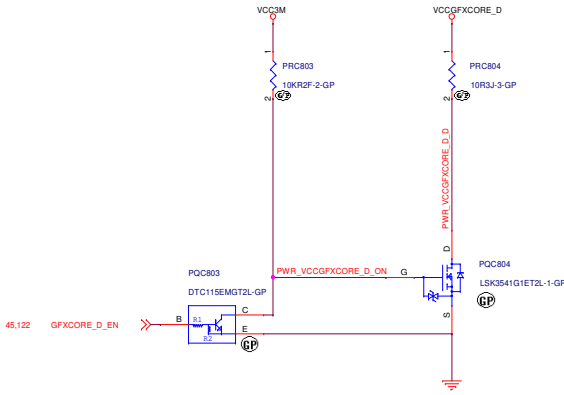
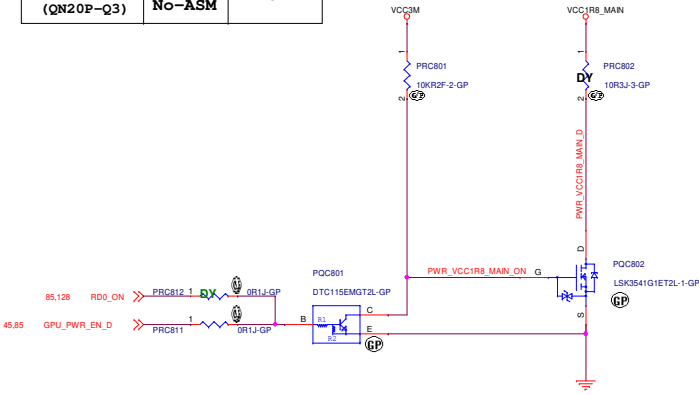
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	PRC811	PRC812
GB5-128 (QN20P-Q1)	ASM	No-ASM
GB5B-128 (QN20P-Q3)	No-ASM	ASM



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Title <b>DISCHARGE Circuit VIDEO</b>		
Size A2	Document Number <b>Cheetah</b>	Rev <b>-1</b>
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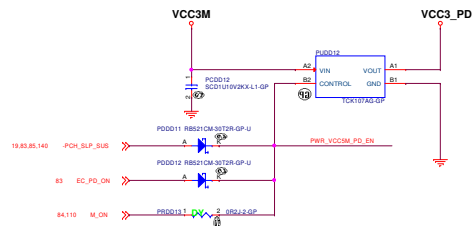
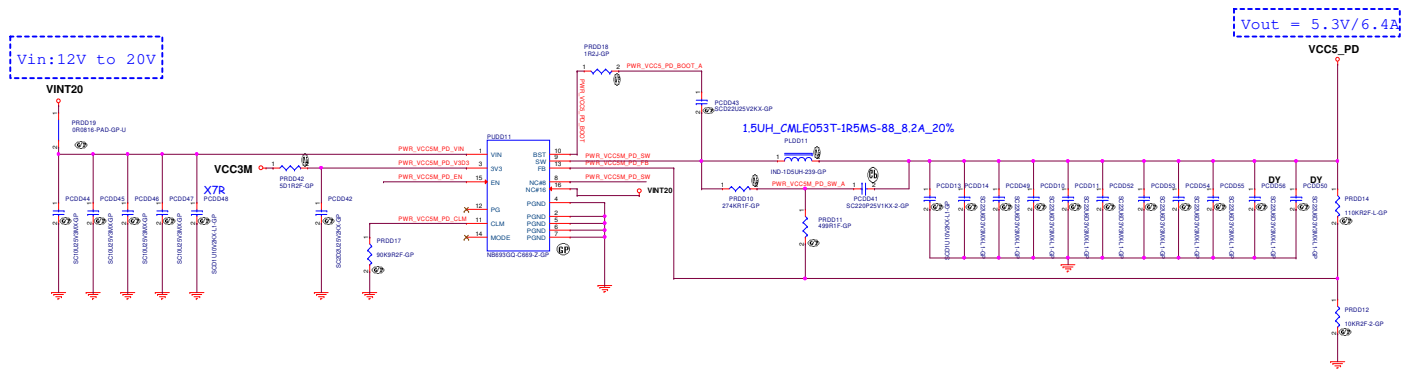
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<div>緯創資通</div>		<div>Wistron Corporation</div>	
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Size C	Document Number <b>Cheetah</b>		Rev <b>-1</b>
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TABLE of PLDD11			
	VENDOR	P/N	Wistron P/N
1st	Cyntec	CMLE053T-1R5MS-88	068.1R510.1751
2nd	Sumida	0530CDMCCDS-1R5MC	068.1R510.1851



VER1.10







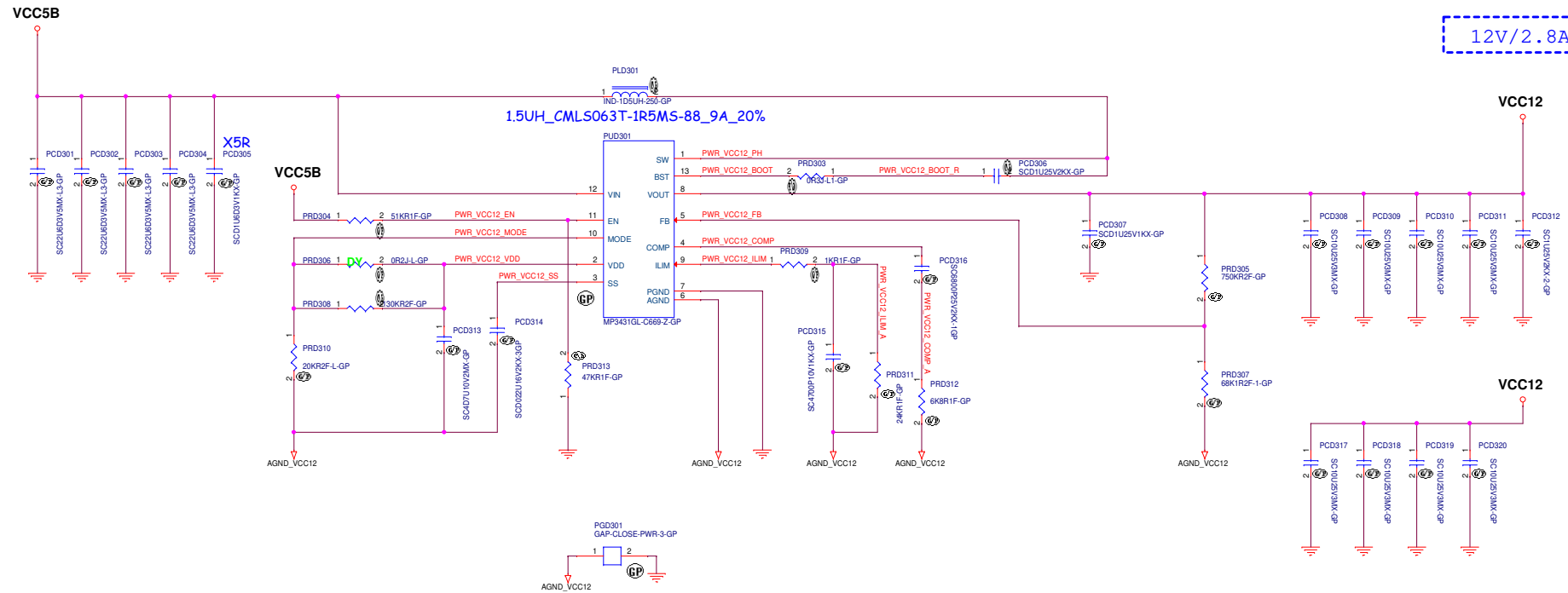
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<div>緯創資通</div>		<div>Wistron Corporation</div>	
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TABLE of PLD301			
	VENDOR	P/N	Wistron P/N
1st	Cyntec	CMLS063T-1R5MS-88	068.1R510.2381
2nd	Sumida	0630CDMCDSD-1R5MC	068.1R510.1871





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Size C	Document Number <b>Cheetah</b>		Rev <b>-1</b>
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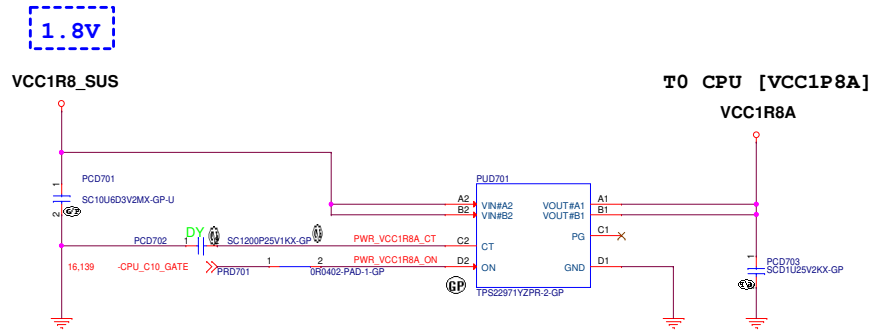


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refer schematic used TPS22971YZPT . Package Qty 250 PCS  
TPS22971YZPR Package Qty 3000 Pcs

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<b>緯創資通</b>		<b>Wistron Corporation</b>	
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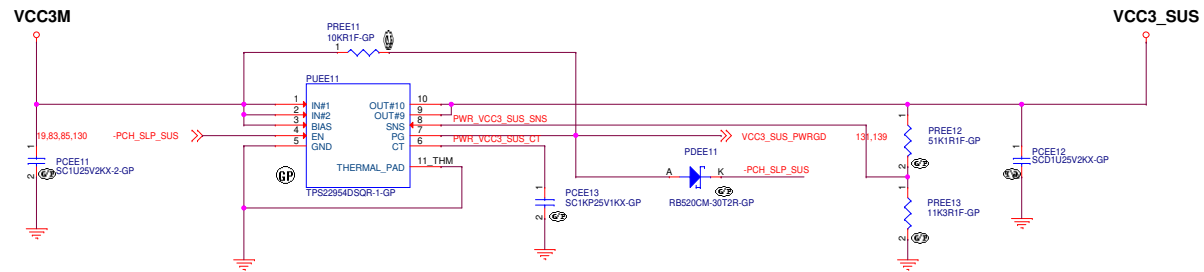
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<div>緯創資通</div>		<div>Wistron Corporation</div>	
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Size C	Document Number <b>Cheetah</b>		Rev <b>-1</b>
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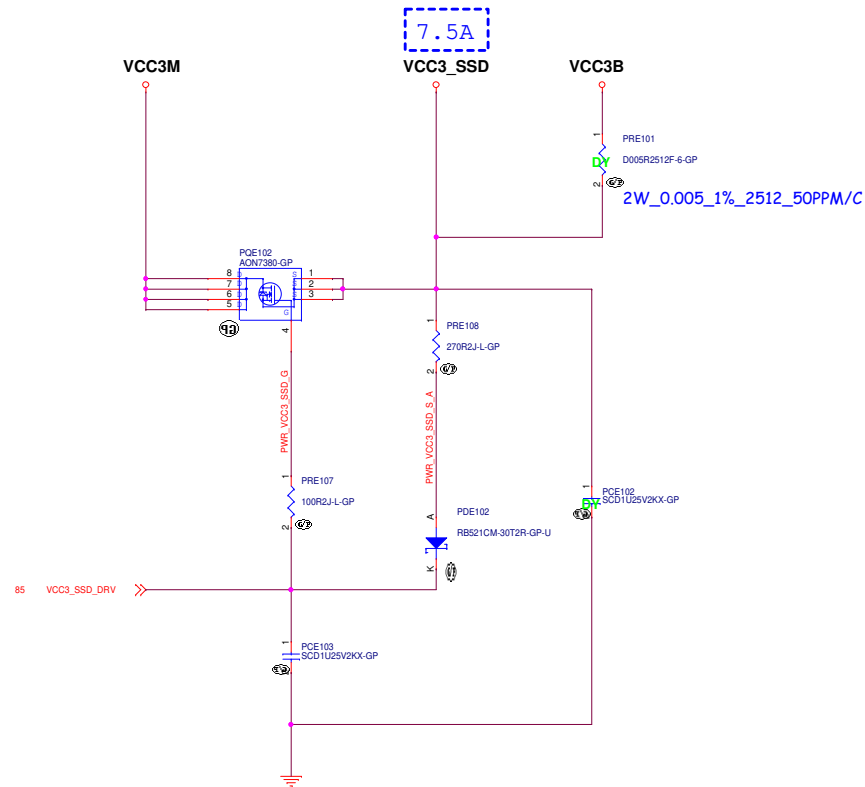
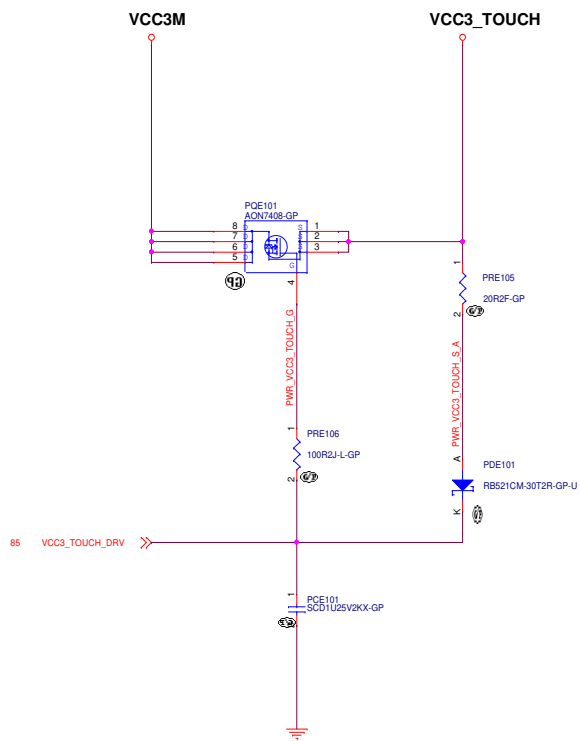




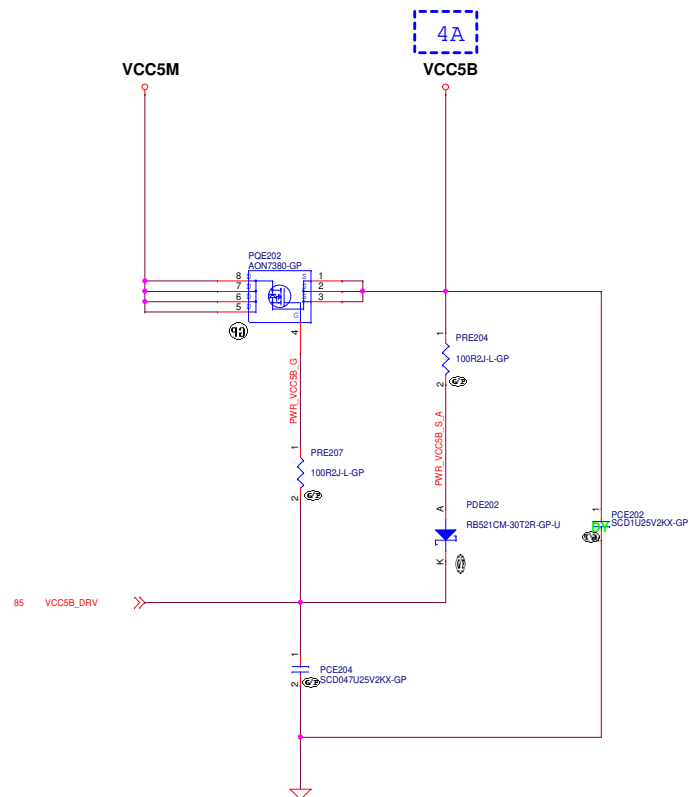
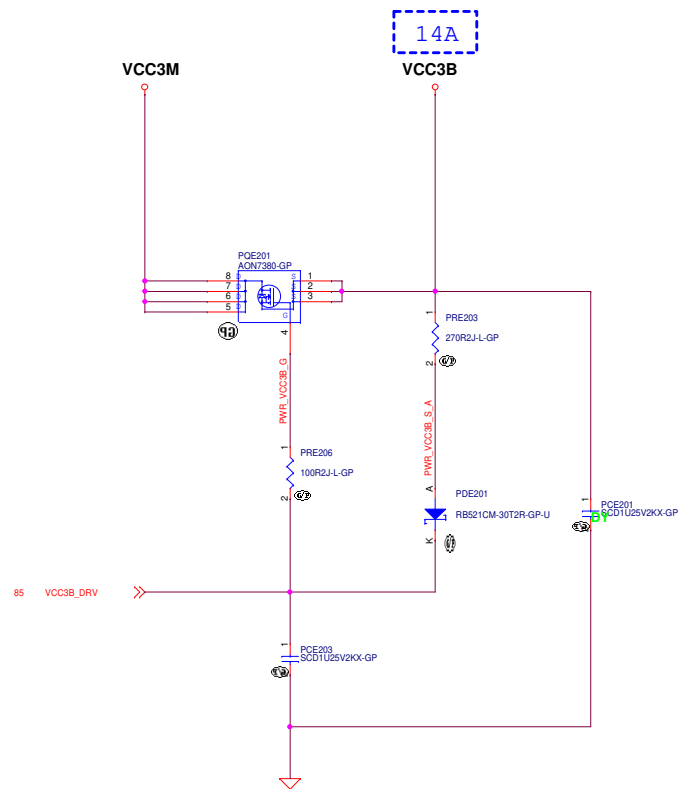
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<b>緯創資通</b>		<b>Wistron Corporation</b>	
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Size	Document Number	<b>Cheetah</b>	Rev
C			<b>-1</b>
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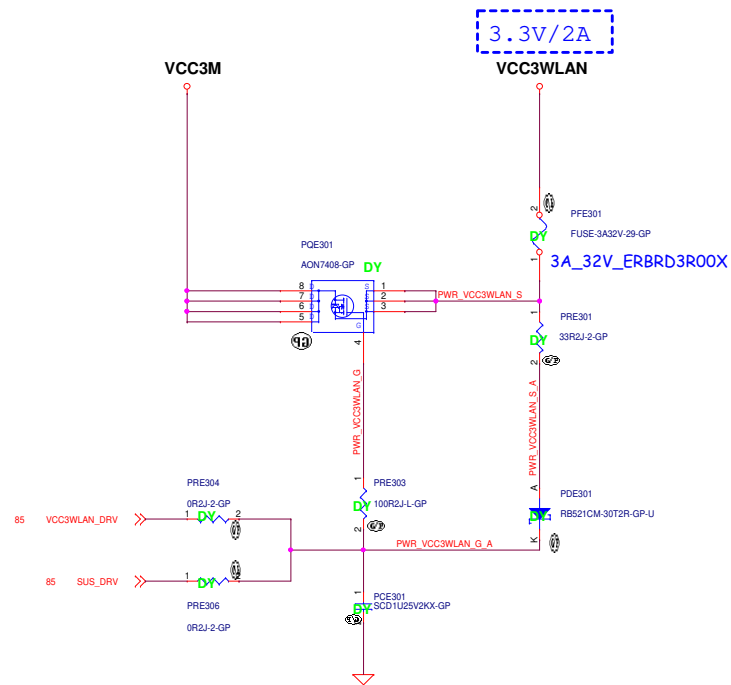




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<b>緯創資通</b>		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
File <b>LOAD SW B</b>			
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To be updated

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Custom	Cheetah		-1
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